

**Bilal Ahmad**

# **Wide Band Gap Power Semiconductor Devices and their Applications**

**School of Electrical Engineering**

Master's Thesis submitted in partial fulfilment of the requirement for the degree of Master of Science in Technology.  
Espoo

**Thesis supervisor:**

Professor Jorma Kyyrä

**Thesis instructor:**

Professor Jorma Kyyrä

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| School of Electrical Engineering   | <b>ABSTRACT OF THE MASTER'S THESIS</b> |
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| <b>Supervisor:</b> Professor Jorma Kyyrä   |  |
| <b>Instructor :</b> Professor Jorma Kyyrä  |  |
| <p>DC power supplies are being widely used in almost every modern day appliance. Basic DC power supply should only consist of AC/DC rectification unit with bulk capacitor. But irregular current drawn by rectifier pollutes the power system. Standards related to power quality puts a limit on harmonics that are being injected by a device into power system. To comply with standards Power factor correction (PFC) circuits are employed with rectification unit. Addition of an extra unit, puts a limit on overall efficiency of power supply. Advent of Wide Band Gap (WBG) power semiconductor devices have provided us with the opportunity to improve the efficiency of existing electronic circuits with relatively simple control schemes. According to recent research, it has been forecasted that GaN based devices are ideal choice for medium voltage and high speed applications. However, SiC based devices are estimated to take over high voltage applications.</p> <p>Conventional PFC circuit based on bridged CCM average current controlled Boost converter was chosen for this study. Simulation was made to compare the performance of GaN, SiC and Si based switches. Results from simulation revealed that 38% reduction in switching losses can be achieved by using GaN HEMT instead of Si MOSFET. Practical evaluation was performed on Transphom Totem Pole PFC and All in One Power supply. Both of these devices are based on GaN HEMTs. Totem pole PFC is the major breakthrough achieved by GaN HEMT in the field of PFC circuit. Very low reverse recovery of switches made it possible to implement this circuit with very high efficiency for high power applications. 94% efficiency was observed during evaluation of DC power supply, which validates the claim of superior performance of WBG devices.</p> |  |
| <b>Keywords:</b> Wide Band Gap, Power Factor Correction ,HEMT, Totem Pole PFC, All in One Power Supply   |  |

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## Chapter 1. Introduction:

Worldwide generation of electricity counts as 43% of overall energy and 45% of total electrical energy is being consumed by electrical motors. It is being estimated that by simply employing wide band gap (WBG) switches instead of conventional Silicon IGBTs, efficiency of motor drives can be increased by 20 to 30% (Hostetler, Alexandrov et al. 2014). Highly efficient WBG devices make these power electronic devices highly adaptable for green energy initiations.

Power Electronics devices have become necessary components of power systems. Emerging electronic appliances including chargers for note books, Mobile Phones and Uninterruptible power supply (UPS), frequency converters, require more power conditioning devices. Internal losses of power conditioning devices put an extra load on National Grid. With depletion of conventional sources of energy and transferring towards green sources of energy, device efficiency holds an important position in deciding the future of particular technology.

Introduction of WBG devices have not only improved the quality of power applications, they have made possible many power electronics circuits that were not possible to realize with silicon devices. One such circuit (totem Pole Power factor correction Circuit) will be discussed in detailed in later chapters.

For last few years, Wide Band Gap (WBG) based Power devices are well promoted for their superior properties over Silicon Power devices. With availability of WBG power devices by many different suppliers, the cost has been reduced by many folds. Reduction of cost has motivated many designers to use these power devices and explore their applications.

With introduction of switch mode power supplies (SMPS), irregular current drawn by SMPS pollutes the power system. Standards related to power quality puts a limit on harmonics that are being injected by a device into power system. To comply with standards Power factor correction (PFC) circuits are employed with rectification unit. Addition of PFC in Switch Mode circuit puts a limit on overall efficiency.

With emerging applications of Power Electronics, power density has become critical in design of converters. With introduction of Wide Band Gap devices, it has become possible to operate at very high switching frequencies and hence reduce the size of passive elements to increase the power density. But the presence of bulk capacitor at output to meet the holdup requirement puts a limit on circuit efficiency and thermal management design. Resonant LLC converter with Zero voltage Switching can greatly

reduce the requirement of holdup time capacitor, and it becomes the most favorable topology because of its high efficient and wide voltage operation range (Bing Lu, Wenduo Liu et al. 2006).

Main motivation behind writing this thesis was to investigate and summarize the current status of wide band gap semiconductor devices. Structure of Thesis can be described as:

Chapter 2 includes the detailed analysis of WBG power semiconductor devices. Potential applications of these switches are also being explored in this chapter.

Chapter 3 gives the detailed introduction of different PFC circuits, their applications and draw backs of different PFC circuit topologies. Later section of this chapter explains the design procedure and LTspice simulation of Single Phase Bridged PFC circuit. Results of simulation are also being presented in the same chapter.

Chapter 4 is about the brief introduction of Resonant LLC circuits. Half Bridge LLC circuit is being discussed in detail in this chapter.

Chapter 5 includes experimental results obtained from performance analysis of Transphorm Totem Pole PFC Circuit and Transphorm All in One power Supply.

Chapter 6 will present a brief conclusion and recommendations for future work in this project.

## Chapter 2. Wide Band Gap (WBG) Semi-Conductor Devices:

### 2.1 Why Wide Band Gap Devices Power Semi-Conductor Devices?

Recently there has been tremendous achievements in the silicon industry. But with increasing high demands of lower switching losses, higher switching speeds, higher power densities, it seems to appear that silicon industry has almost reached to its saturation point. Silicon semiconductor devices put restriction to many features of power electronics devices including switching speeds, power density and operation at high ambient temperatures. Immensely hard efforts are required to get more breakthroughs in silicon power devices.

MOSFETs are the most widely used Semiconductor device in medium voltage range Power electronics applications. History of MOSFETs goes back to 1976, when they were first introduced as replacement of Bipolar Junction Transistors (BJTs). MOSFETs showed far better performance than BJTs and hence become the major contenders to be used in vast commercially available AC/DC converters (Lidow, Strydom et al. 2014). For over three decades there had been a continuous improvement in device efficiency, power density and circuit topologies for MOSFETs to meet the ever increasing demand and quality of electrical power. However as mentioned above, Si MOSFET technology has almost reached to its saturation point and in this new millennium researchers could not achieve any major breakthrough in this technology.

Conventional Silicon FET technology puts a limit on performance of devices. Switching losses and conduction losses are the two major types of losses that occur in every semiconductor device. As their name implies switching losses include the losses occur during switching ON or turning off of the device. Whereas conduction losses occur when the device is conducting.

Conduction losses are simple  $I^2R_{DS}$ —losses which occur across the drain to source resistance of device. One solution to reduce the  $R_{DS}$  is by using various switches in parallel. Indeed this approach will reduce the equivalent resistance but paralleling of devices means more capacitance and hence more charge. This will increase the switching losses of device at high switching frequencies (International Rectifier 2015). Performance influencing factors including switching speed, reverse recovery characteristics and thermal characteristics depend upon the material characteristics as well as on fabrication technology. Hence, designers need to find an optimal approach to enhance the overall performance.

However Wide Band Gap (WBG) materials that include Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond can provide us with alternative approach to achieve major breakthroughs in the field of Power electronics (Millan, Godignon 2013). These



devices are more attractive than silicon ones, as they have higher break down voltage, higher thermal conductivity, greater energy band gap and have better carrier mobility (Chow, Tyagi 1994). Theoretically WBG power devices are many times superior to their counterpart Si power devices. However practically things are pretty much different, as there are many practical issues that are yet to be resolved. Especially epitaxial growth and device fabrication technologies are yet to get matured and reliable.

## 2.2 Properties of WBG Semiconductor Materials:

Future of Power electronics industry lies in WBG semiconductor devices. WBG semiconductor materials can be defined as materials with band gap of more than 2.2 eV (Yoder 1996). In this section we will discuss about the features of WBG devices that make them superior to its competitors.

Out of all WBG materials, diamond has the largest band gap and hence largest breakdown strength. Band gap of SiC and GaN have same level, but surely larger than that of Si. Break down voltage of a diode can be expressed as (Ozpineci, Tolbert et al. 2003)

$$V_B = \frac{\epsilon_r E_c^2}{2qN_d} \quad (2-1)$$

Where  $q$  is charge on electron and  $N_d$  is doping level. Author of (Ozpineci, Tolbert et al. 2003) calculated the breakdown voltage of diode for different materials and normalized the results to the break down voltage of Si diode, Figure 1 presents the results:

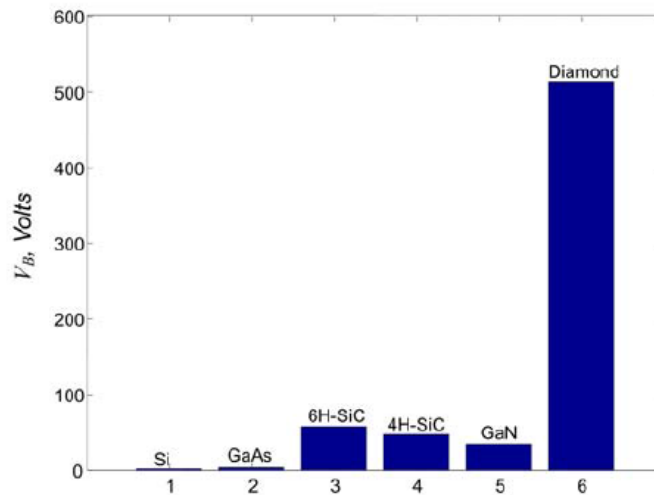


Figure 1: Break down voltage of Power Device with different Materials (Ozpineci, Tolbert et al. 2003)

These results were obtained for same level of doping. As we mentioned above diamond being with the largest Band gap has 500 times more break down strength than Si. SiC and GaN are also way ahead of Silicon Power Devices.

4H-SiC and 6H-SiC are basically a polymorphs of SiC. We will not go into the physics of material. However details can be found in (Ching, Xu et al. 2006)

Electric field endurance of semiconductor device depends upon the thickness of P-N junction.  $E_{MAX}$  being the maximum electric field that a device can with stand before it get destroyed by break down of junction, the minimum width of P-N junction can be given by this equation (Bergman 1996):

$$W > \frac{2V_B}{E_{Max}} \quad (2-2)$$

Where  $V_B$  is break down voltage and  $W$  is thickness of P-N junction.

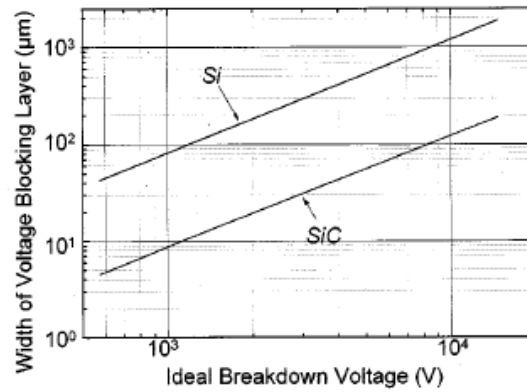


Figure 2: Si vs SiC Break down Voltage (Hefner Jr, Singh et al. 2001)

SiC has almost 10 times more  $E_{MAX}$  than that of Si, which means that to with stand the same level of voltage, SiC device would be 10 times thinner than that of Si device(Bergman 1996) . This property of WBG semiconductor devices has led to achievement of major breakthrough in overall Power density of converters. SiC is the most mature and number one contender in the list of materials which can replace Silicon from Power electronics industry. SiC power devices has almost 10 times more dielectric strength and 5 times more thermal conductivity than that of Si power devices (Yoder 1996). Break down strength of SiC Power semiconductor devices make them to stand ahead of its competitors. SiC has break down strength in the range of kV, however silicon (Si) devices are limited to range of 500 to 1000 V (Bergman 1996).

Thermal conductivity of Wide band gap semiconductor devices is many times higher than that of Silicon. Apart from it, existence of Wide band gap will lead to enormous

thermal stability of devices as well. For specific temperature, leakage current of WBG semiconductor devices would be 10-14 times lesser than that of conventional semiconductor devices (Yoder 1996).

Thermal conductivity of semiconductor devices can be compared as shown in **Error! eference source not found.** (Yoder 1996):

*Table 1: Thermal Conductivity Comparison*

|  | Silicon | 4H-SiC | GaN | Diamond |
|--|---------|--------|-----|---------|
| Thermal Conductivity<br>(Wcm <sup>-1</sup> K <sup>-1</sup> ) | 1.5     | 4.9    | 1.3 | 22      |

Operating temperature is critical parameter in deciding the performance and life of the device. Power devices in converters are subjected to instances which increase the temperature in surroundings of power switch e.g. unclamped inductive load. Switching operation of power device at rated current and bus voltage acts as the major source of heat generation. This high temperature has adverse effects on reliability issues. But because of size reduction of technology it is no longer possible to insert more heat sinks or any forced cooling mechanism including cooling fans. It is no longer possible for conventional silicon power devices to give the desired results in environment with elevated temperature. High electron mobility, higher bang gap, higher break down voltage make Wide Band gap power semiconductor devices superior to silicon devices (Trivedi, Shenai 1999). Especially SiC and diamond are showing many promising results, though there is a huge room for improvement in this technology.

### 2.3 Technology Status of Wide Band Gap (WBG) Semi-Conductor Devices:

During recent years technology of WBG devices has evolved itself to a level where it can be considered as potent replacement of Si technology.

In this section we will talk about the recent developments in SiC and GaN power devices.

#### 2.3.1 Silicon carbide (SiC) Devices:

Silicon carbide devices have revolutionized the whole field of Power electronics in last decade. High dielectric strength, low ON resistance, high power density makes them ideal for switch mode circuits. Outstanding properties of Sic devices make them suitable for high power, high speed and high temperature circuits. Due to keen interest of researchers and potential investors, many improvements have been made

in production of SiC. As a result, 100 mm 4H-SiC substrate and epilayers are readily available (Agarwal 2010).

As mentioned before 4H-SiC is just a polymorph. Silicon carbide has more than 100 polymorphs depending upon the stacking of layers of Si and carbon (C) layers. For example 4H-SiC has hexagonal structure with 4 layer repeat structure. Though there are many polymorphs of SiC, researchers restricted their research to only 3C, 6H and 4H because of their better performance over other polymorphs (Wright, Horsfall et al. 2008). Out of these three 4H showed the more superior properties with band gap of 3.23 eV as compared to 1.12 eV of silicon.

SiC power devices were first introduced in market in 2001. However, issues related to growth of crystal has limit the application of SiC devices. Since then there has been a lot of development in fabrication process. Many processes including rapid thermal annealing of metal layers, stepper lithography for 3" which were not among standard process for the production of Si devices, have now added in the list of standard process for fabrication of SiC devices (Treu, Rupp et al. 2006).

First SiC device that took the market by storm was SiC diodes. Since its early days, tremendous amount of work has been done in order to improve the performance of diodes. With the development of technology other devices including BJTs, MOSFETs came in to the market as well. We will have a thorough look that where does each device stand in the market and how satisfactory its performance has been over the past years.

| Suppliers                            | Epi Substrate | Wafer Size    | Transistor Type                              | Maximum Voltage (V) | Diode       | Maximum Voltage (V)       |
|--------------------------------------|---------------|---------------|--|---------------------|-------------|---------------------------|
| Avogy                                | GaN           | 2-in (50 mm)  | E-mode <sup>1</sup> vertical JFET            | 1,200               | Schottky PN | 600 (Schottky) 1,700 (PN) |
| Efficient Power Conversion           | Si            | 6-in (150 mm) | E-mode FET                                   | 450                 | Schottky    | 600                       |
| Exagan                               | Si            | 8-in (200 mm) | —  | 1,200               | —           | —                         |
| Fuji Electric                        | Si            | —             | —  | —                   | Schottky    | 600                       |
| Fujitsu Semiconductor                | Si            | 6-in (150 mm) | —  | —                   | —           | —                         |
| GaN Systems                          | Si            | 6-in (150 mm) | E-mode HEMT                                  | 650                 | —           | —                         |
| International Rectifier <sup>2</sup> | Si            | 6-in (150 mm) | Depletion-mode HEMT <sup>3</sup>             | 600                 | —           | —                         |
| microGaN GmbH                        | Si            | 6-in (150 mm) | Heterostructure FET <sup>3</sup>             | 600                 | —           | —                         |
| NXP Semiconductor                    | Si            | —             | —  | —                   | Schottky    | 650                       |
| Panasonic                            | Si            | 6-in (150 mm) | Normally off gate injection transistor (GIT) | 600                 | —           | —                         |
| POWDEC K.K.                          | Sapphire      | —             | Polarization Super-junction FET              | 600                 | Schottky    | 600                       |
| RF Micro Devices                     | SiC           | 4-in (100 mm) | Source switched FET                          | 650                 | —           | —                         |
| Sanken Electric Co., Ltd.            | Si            | N/A           | Normally off FET                             | 600                 | Schottky    | 600                       |
| STMicroelectronics                   | Si            | 6-in (150 mm) | E-mode HEMT                                  | 200                 | —           | —                         |
| Transphorm                           | Si            | 6-in (150 mm) | HEMT <sup>3</sup>                            | 600                 | Schottky    | 600                       |

Source: How2Power Today.  
<sup>1</sup>Enhancement-mode. <sup>2</sup>Acquired by Infineon Technologies. <sup>3</sup>Offered in normally off cascode form.

Figure 3: Suppliers of SiC Power Devices (Bindra 2015)

With increase in production and application utilization of SiC power devices, their market reached to the level of 96 Million USD in 2013 and is expected to reach 360 Million USD by 2020 (Bindra 2015).

### 2.3.1.1 SiC Diodes:

Power diodes have important place in all power electronic circuits and it was being expected by researchers that Power diodes made up of SiC will show promising results. High blocking voltage and low electron mobility of SiC resulted in 10 times reduction in size and almost 100 times increase in doping for same blocking voltage (Singh, Cooper et al. 2002). The main advantages that 4H-SiC diode have over Si diodes include (Treu, Rupp et al. 2006):

- Almost 2 times lesser ON state resistance of SiC based Schottky Diodes, and hence less ON state voltage drop.
- Thinner epitaxial layers result in 30 times more switching speeds than that of Si diodes.

We will restrict our discussion only to performance and status of this technology. However if reader is interested in detailed fabrication of diodes, it can be found in (Singh, Cooper et al. 2002).

SiC rectifiers can be classified in to three types (Hefner Jr, Singh et al. 2001):

- Schottky diodes for applications with very high frequencies with comparatively high leakage current.
- PiN diodes with low leakage current but restricted switching frequencies because of reverse recovery characteristics.
- Merged PiN Schottky (MPS) diodes that exhibit the characteristics of both PiN and Schottky diodes. These diodes are also classified as Junction Barrier Schottky (JBS) diodes.

Schottky diodes have been discussed a lot before.

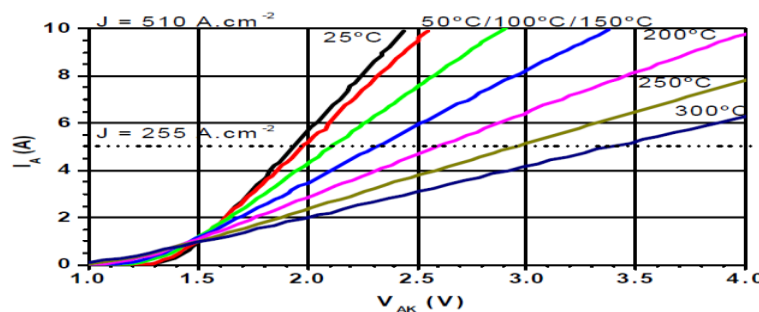


Figure 4: Forward Characteristics of 4H-SiC Schottky diode (Brosselard, Jordà et al. 2007)

Schottky diodes exhibit the best forward characteristics, with minimum forward drop among all type of diodes. However, their reverse characteristics make them less desirable for application with high blocking voltage and raised operating temperature.

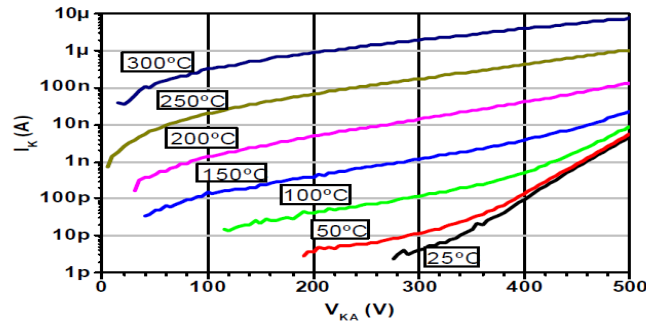


Figure 5: Reverse Characteristics of 4H-SiC Schottky diode (Brosselard, Jordà et al. 2007)

Tunnel effect in Schottky diodes lead to 10 times more leakage current than SiC JBS diodes (Brosselard, Jordà et al. 2007). However, leakage current is still many times lesser than that in conventional silicon diodes.

Conventional silicon P-i-N diodes are restricted to application with switching frequencies less than 50 kHz with operating temperature of less than 150 °C. This restrict the application of these diodes in many intelligent electronic circuits including Power conditioning circuits ,intelligent machinery and circuits for energy storage and pulsed power. 4H-SiC P-i-N rectifier makes the operation possible at elevated temperatures, at very high switching frequencies. SiC P-i-N rectifier with blocking voltage of 5.5 kV was first introduced in (Singh, Irvine et al. 1998). For current density of 100A/cm<sup>2</sup> forward drop of 5.4 V was being observed.

SiC PiN diodes have following advantages over conventional Silicon diodes.

- Forward drop of SiC PiN diodes is comparable to stacked Si power diodes (Hefner Jr, Singh et al. 2001).
- Much higher switching frequencies.
- Better performance at elevated temperatures (Hefner Jr, Singh et al. 2001).

5kV SiC PiN diode was being studied in (Hefner Jr, Singh et al. 2001).

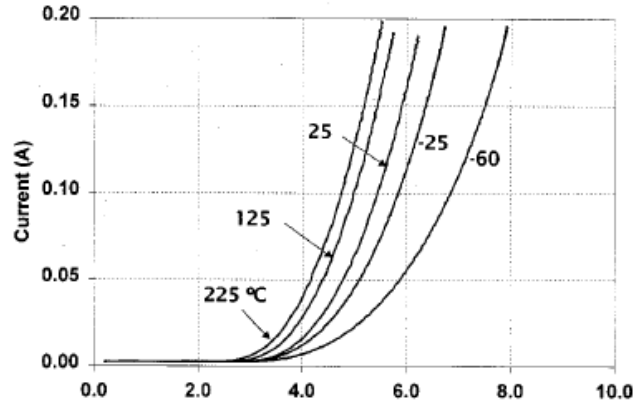


Figure 6: temperature Dependence of 5kV SiC PiN diode (Hefner Jr, Singh et al. 2001)

Higher ON state voltage was observed because of higher band gap in sic than in Si. Reverse recovery characteristics were investigated by the author for Boost Converter.

|                 | <b>Repetitive<br/>Peak Reverse<br/>Voltage<br/><math>V_{RRM}</math> (V)</b> | <b>Forward<br/>Voltage<br/>Drop<br/><math>V_f</math> (V)</b> | <b>Reverse<br/>Recovery<br/>Time<br/><math>t_{rr}</math> (ns)</b> |
|-----------------|---|--|---|
| SiC PiN         | 5000  | 5.7  | 6   |
| VMI X50FF3      | 5000  | 12.5   | 30  |
| VMI X20FF3      | 2000  | 7.5  | 30  |
| VMI 1N6523      | 3000  | 5.0  | 70  |
| VMI 1N6524      | 4000  | 7.0  | 70  |
| Philips BYX105G | 5000  | 10.9   | 600   |
| Philips BYX106G | 5000  | 12.7   | 350   |
| Philips BYX107G | 5000  | 15.8   | 175   |
| Philips BYX108G | 5000  | 27.7   | 50  |

Figure 7: Comparison SiC PiN Diode vs Si Diodes (Hefner Jr, Singh et al. 2001)

Author of (Hefner Jr, Singh et al. 2001) calculated the data for Si from different vendors. SiC was tested at 60 A/cm<sup>2</sup>, however Si devices were tested at 20 A/cm<sup>2</sup> because of their thermal limitation.

Under high reverse voltage and elevated temperature, SiC Schottky diode suffers from leakage current. JBS diode provide solution to leakage current in Schottky and high

forward drop problem in PiN diodes by keeping almost zero leakage current with forward voltage drop of less than 3 V.

To keep the forward voltage drop in permissible range it would be required that only Schottky region conducts. As forward drop depends upon the resistance of drift region, metal-SiC barrier height and relative area of Schottky vs P<sup>+</sup> regions (Singh, Ryu et al. 2000). As P<sup>+</sup> will not be conducting during forward bias condition, hence the current density in Schottky region will be greater than the current density of entire device. Metal-SiC barrier height is low enough to reduce the ON state drop while large enough to completely pinch off the diode under reverse bias condition. Under high reverse voltage and elevated temperature, implanted p<sup>+</sup> regions completely pinch off the leakage current arising from Schottky regions.

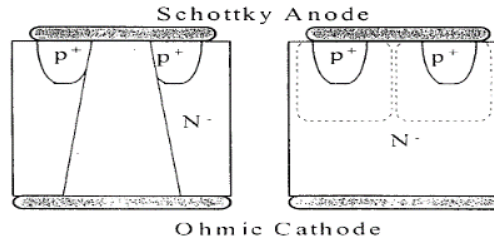


Figure 8: Cross-section of JBS Diode (Singh, Ryu et al. 2000)

Detailed analysis of JBS diode was carried out by (Hefner Jr, Singh et al. 2001). Forward and reverse characteristics of JBS, Schottky and PiN diode were compared by the author. JBS diode showed forward characteristics almost similar to Schottky diode with forward drop of 3.1V for high ON current of 4A which gives the specific ON resistance of only 10 mΩcm<sup>2</sup>. However, as compared to Schottky diode negligible increase in forward drop of JBS diode was observed because of introduction of p<sup>+</sup> regions.

Reverse characteristics of JBS and PiN diodes were found similar. Leakage current of 50 μA was measured for a blocking voltage of 610 V.

Another study made by (Fedison, Ramungul et al. 2001) revealed the similar results for implant JBS diodes. Author measured forward drop of 4.1 V at room temperature and reduced to 3.3 V at 250 °C for current density of 100 A/cm<sup>2</sup> which gives the specific resistance of 2.7 mΩcm<sup>2</sup> which reduces to 2.35 mΩ at 250 °C.

Reverse characteristics of JBS diode revealed leakage current of less than 1μA for reverse voltage of 4.5kV.



Cree has been reported with best Line of JBS diodes. 1.2kV/75A and 1.2kV/100A SiC JBS diodes have already been developed. Forward characteristics revealed the forward drop of 1.77V at 100A and leakage current of 250 $\mu$ A for blocking voltage of 1.33kV. 10kV 20A JBS diodes have also been developed. Forward characteristics are presented in Figure 9. Leakage current of 80 $\mu$ A was calculated for reverse voltage of 10kV (Callanan, Agarwal et al. 2008).

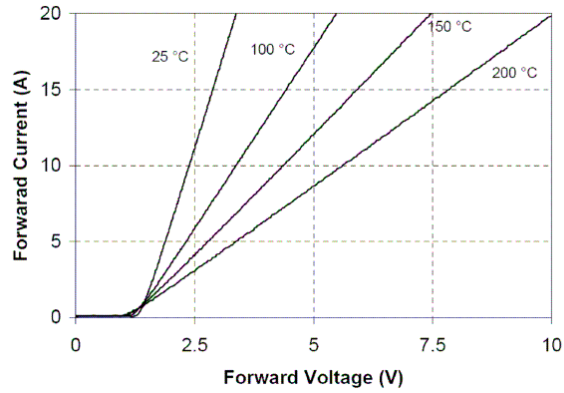


Figure 9: Forward characteristics of 10kV, 20A SiC JBS Diode (Callanan, Agarwal et al. 2008)

Switching characteristics were studied by author of (Brosselard, Jordà et al. 2007). Measurements were done on Buck converter.

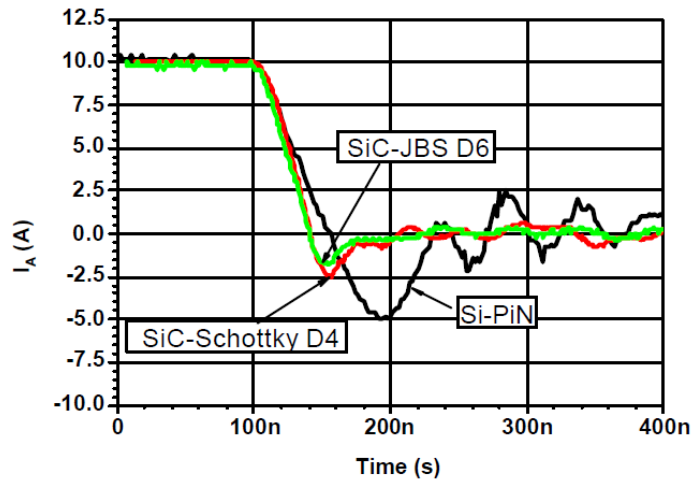


Figure 10: Turn off current waveforms (Brosselard, Jordà et al. 2007)

#### 2.3.1.2 SiC MOSFETs:

Conventional silicon MOSFETs have many limitations that they inherit from material properties of Silicon. Blocking voltage and specific ON resistance are two vital properties of MOSFET. Thickness and doping level of drain drift region are the factors that influence above mentioned properties of MOSFET (Palmour 1996). Increase in

thickness of drift region and reduction of doping level results in higher blocking voltage with higher ON resistance. These problems motivated many researchers to develop new models of power MOSFETs.

Higher band gap of silicon carbide makes it possible to develop MOSFET substrate several times thinner and with higher doping than that of silicon MOSFET with same blocking voltage and lesser specific ON resistance. This makes it possible to have SiC MOSFETs for the voltage range of kilo volts. SiC UMOSFETs or Trench MOSFETs were the first SiC power MOSFETs that got researchers attention. However UMOSFET suffers from low breakdown voltage and lower inversion layer channel mobility makes them unattractive for many applications. After UMOS another SiC MOSFET planar structure was being introduced with better inversion layer mobility known as double implanted Power MOSFET (DIMOS) (Shenoy, Cooper et al. 1997).

In order to solve body diode degradation problem and extra expense added due to addition of Schottky Diode in parallel to DMOS, another SiC based device DioMOS is used. In DioMOS an extra high doped N-type epitaxial layer is added beneath oxide layer of gate. This additional layer reduces the potential barrier for the electrons at reverse conduction to 0.8 eV. 100 A/1200 V SiC DioMOS power Module is presented in (Watanabe, Hozumi et al. 2014). Concept behind this technology can be understood by Figure 11:

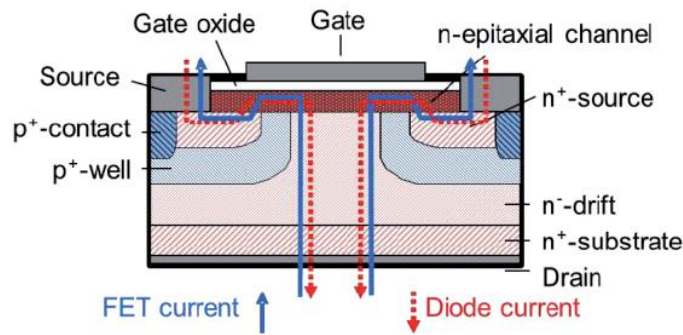


Figure 11: SiC DioMOS (Watanabe, Hozumi et al. 2014)

By increasing the doping concentration of N-type channel we can further reduce the forward drop of body diode or channel diode. This technology also reduces the parasitic inductance from the circuit that arises due to connection of anti-parallel diodes. This power module has threshold voltage of 3.9 V with forward drop of 0.8 V in body diode. Detailed switching characteristics can be found in (Watanabe, Hozumi et al. 2014)

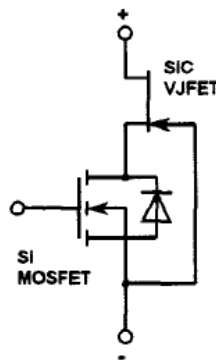
In May 2015 Cree introduced a new class of 900V SiC that are ideal for PFC circuits and LED drivers. In this structure they have further increased the doping level in

blocking layer to reduce the ON resistance. This MOSFET gave the ON resistance of  $2.3 \text{ m}\Omega\text{-cm}^2$ , which is the lowest ON resistance for any 900V MOSFET available in the market (Schupbach 2015). For a temperature rise from  $25^\circ\text{C}$  to  $150^\circ\text{C}$ , only 46% increase in ON resistance was observed which is 3 times lesser than CoolMOS technology.

With emerging applications of SiC MOSFET there has been tremendous improvement in reliability and characteristics of power devices. Cree is about to launch 1200V SiC MOSFET with ON resistance of  $25 \text{ m}\Omega$ . 1700V SiC MOSFET is all set to be released later in 2015 (Bindra 2015). It has also been demonstrated by researchers that in upcoming few years it will be possible to fabricate SiC MOSFET with blocking voltage of 10 kV. However SiC MOSFETs still have many reliability and cost effectiveness issues that are hurdles in their way to take over the power electronics industry.

### 2.3.1.3 SiC JFETs:

With Low ON resistance and high blocking voltage, SiC has introduced new prospects to the field of Power Electronics. SiC JFETs offer better thermal performance than Si MOSFETs with higher switching frequencies. One main disadvantage is that JFETs are inherently Normally ON devices, which makes them impractical for many applications. In order to use normally ON JFETs, significant modification will be required in driver circuits and switch protection circuits. One option is to use them in cascade configuration. Normally ON JFETs are connected in series with normally off Low voltage Si MOSFET and switch will be controlled through the gate of Si MOSFET.



*Figure 12: Normally off SiC cascoded JFET (Rodriguez Alonso, Fernandez Diaz et al. 2014)*

As we can see in Figure 12 gate to source voltage of SiC JFET is basically source to drain voltage of Si MOSFET. So when Si MOSFET will be turned ON with positive gate voltage, drain to source voltage of Si MOSFET will reduce below the pinch off voltage of SiC JFET and hence JFET will be turned ON. Similarly, when Si MOSFET will be switched off drain to source voltage will increase to pinch off level of JFET, resulting

in switching off of JFET. Complete waveforms and detailed analysis of switching behavior of cascaded structure is explained in (Rodriguez Alonso, Fernandez Diaz et al. 2014)

Normally off-SiC JFETs with rating of 1200V have been reported to be available in market by several vendors (Hostetler, Alexandrov et al. 2014). Efforts are still being made for WBG devices with higher power rating, as high switching speeds of SiC devices increases the power density and cost of magnetic materials.

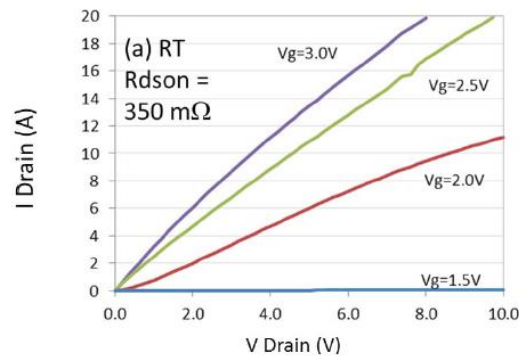


Figure 13: Forward characteristics of 6.5kV JFET (Hostetler, Alexandrov et al. 2014)

Figure 13 shows the forward characteristics of normally off 6.5 kV JFET at room temperature. Gate Threshold voltage of 1.7 V was observed for this JFET (Hostetler, Alexandrov et al. 2014).

### 2.3.2 GaN Power Devices:

Five major characteristics of GaN devices includes: high Dielectric strength, High operating temperature, high current density, high switching speed and low-on resistance. These characteristics enable GaN devices to have 10 times more break down strength than that of Silicon devices. Exceptional Electron Mobility makes GaN perfect choice for unipolar devices .Apart from all other superior material properties, thermal coefficient of expansion (CTE) of GaN is very well suited for the ceramic material that is being used a packaging material for semiconductor devices. Low charge storing capability of GaN, makes it possible to develop power devices capable of being switched in RF range with very high efficiencies. High switching speeds with reduced transition periods reduces switching losses to increase the overall efficiency with minimal or almost no requirement of heat sinks or special cooling fans.

With emergence of GaN in power devices, it becomes possible to achieve devices with zero recovery characteristics. Zero reverse recovery of GaN HEMT devices solved the problem of realization of Totem pole PFC.

However, fabrication techniques for GaN power devices needs modification to make this technology cost effective.

With emerging sectors, where GaN Power devices can have exceptional results, there have been dozens of supplier that are supplying various GaN power devices.

| Suppliers                            | Epi Substrate | Wafer Size    | Transistor Type                              | Maximum Voltage (V) | Diode       | Maximum Voltage (V)          |
|--------------------------------------|---------------|---------------|--|---------------------|-------------|------------------------------|
| Avogy                                | GaN           | 2-in (50 mm)  | E-mode <sup>1</sup> vertical JFET            | 1,200               | Schottky PN | 600 (Schottky)<br>1,700 (PN) |
| Efficient Power Conversion           | Si            | 6-in (150 mm) | E-mode FET                                   | 450                 | Schottky    | 600                          |
| Exagan                               | Si            | 8-in (200 mm) | —  | 1,200               | —           | —                            |
| Fuji Electric                        | Si            | —             | —  | —                   | Schottky    | 600                          |
| Fujitsu Semiconductor                | Si            | 6-in (150 mm) | —  | —                   | —           | —                            |
| GaN Systems                          | Si            | 6-in (150 mm) | E-mode HEMT                                  | 650                 | —           | —                            |
| International Rectifier <sup>2</sup> | Si            | 6-in (150 mm) | Depletion-mode HEMT <sup>3</sup>             | 600                 | —           | —                            |
| microGaN GmbH                        | Si            | 6-in (150 mm) | Heterostructure FET <sup>3</sup>             | 600                 | —           | —                            |
| NXP Semiconductor                    | Si            | —             | —  | —                   | Schottky    | 650                          |
| Panasonic                            | Si            | 6-in (150 mm) | Normally off gate injection transistor (GIT) | 600                 | —           | —                            |
| POWDEC K.K.                          | Sapphire      | —             | Polarization Super-junction FET              | 600                 | Schottky    | 600                          |
| RF Micro Devices                     | SiC           | 4-in (100 mm) | Source switched FET                          | 650                 | —           | —                            |
| Sanken Electric Co., Ltd.            | Si            | N/A           | Normally off FET                             | 600                 | Schottky    | 600                          |
| STMicroelectronics                   | Si            | 6-in (150 mm) | E-mode HEMT                                  | 200                 | —           | —                            |
| Transphorm                           | Si            | 6-in (150 mm) | HEMT <sup>3</sup>                            | 600                 | Schottky    | 600                          |

Figure 14: Suppliers of GaN Power Devices (Bindra 2015)

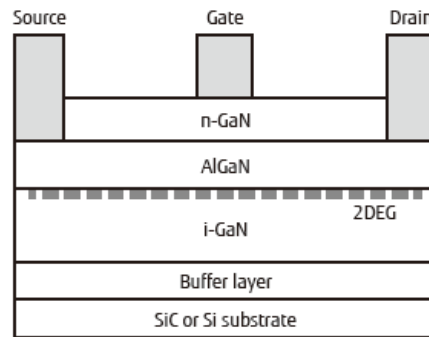
#### 2.3.2.1 AlGaN/GaN High Electron Mobility Transistor (HEMT):

AlGaN/GaN HEMT basically a heterojunction device also termed as Heterojunction Field effect transistor. Ability of GaN to grow on foreign material makes it very attractive for heterojunction devices to achieve very high electron mobility.

AlGaN/GaN High Electron Mobility Transistor (HEMT) are undergoing rapid development and are excellent choice for replacement of Power Si MOSFETs and IGBTs in high switching frequency applications. HEMTs are ideal candidates for high voltage applications because of their high breakdown strength, very low ON resistance and ability to operate at very high frequencies. AlGaN/GaN HEMTs are grown hetero-epitaxially on sapphire or SiC substrate. Despite of their high power densities sapphire substrate suffers from poor thermal conductivity while SiC substrate are not reliable and economically feasible. High quality, large area and cheap Si substrate is considered as an attractive alternative of sapphire and SiC.

However, GaN devices grown on Si substrate, have shown better performance than Silicon devices but still they could not reach the level of same devices grown on SiC and sapphire substrates (Hilt, Knauer et al. 2010).

Basic structure of GaN HEMT is realized by forming a junction between two different semiconductor materials with distinct band gap energies. Such a junction is known as heterojunction (Khan, Bhattarai et al. 1993). Heterojunction of AlGaIn/GaN will lead to the formation of two dimensional electron gas (2DEG) at the interface. Inheritably this electron gas has very high electron mobility of around  $2000\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ . High electron mobility makes possible the realization of power switch with very low ON resistance.



*Figure 15: Basic Structure of GaN HEMT (Joshin, Kikkawa et al. 2014)*

In basic structure of GaN HEMT, shown in Figure 15, Schottky barrier is realized by placing the gate terminal directly over semiconductor material. This structure makes it ideal for high switching low power applications. However in this structure gate voltage is limited to very low voltage of less than 2 V, which makes it impractical for power applications. This problem can be resolved by insulating the gate terminal i.e. by putting dielectric insulation between gate terminal and semiconductor material (Joshin, Kikkawa et al. 2014).  $\text{Al}_2\text{O}_3$  is usually adopted as gate insulating material. But it suffers from electron trap phenomena which results in shifting of gate threshold voltage. Electron trap phenomena will be briefly described in section 2.4. AlOH impurities in  $\text{Al}_2\text{O}_3$  and Ga oxide in  $\text{Al}_2\text{O}_3/\text{GaN}$  interface are responsible for gate threshold shifting. By removing these impurities  $V_{\text{TH}}$  shift can be reduced to 0.25V from almost 2V (Joshin, Kikkawa et al. 2014).

Another, solution to increase the gate threshold voltage is to use normally ON HEMT in cascode configuration with Low voltage Silicon MOSFET. Transphorm developed their 600V GaN HEMT in cascode configuration for normally off operation. TPH3002 by Transphorm that is being used in simulation of PFC circuit in next chapter is 600V GaN HEMT based on cascode configuration.

Goal of all electronic circuits is the realization of most efficient circuit. This will be only be possible if somehow we can make the product of voltage and current zero. But it is impossible to achieve in practical circuits due to finite specific ON resistance of the switch. Moreover, capacitances in the switch makes it impossible to achieve instant switching that will lead to switching losses. In GaN HEMT due to high electron mobility in 2DEG gas, very small ON resistance is being achieved. Low gate capacitance of GaN HEMT makes it ideal device for high speed circuits. Gate charge of GaN HEMT is much smaller than that of Si MOSFET. It means less energy will be stored in junction capacitor that will reduce the switching losses to increase the overall efficiency. But due to its high speed characteristics, it often suffers from ringing effect (Joshin, Kikkawa et al. 2014).

AlGaIn/GaN HEMTs grown on Si or SiC substrates have shown poor thermal conductivity. Study done by (Killat, Montes et al. 2012) revealed that high thermal conductivity of  $240 \text{ W cm}^{-1} \text{ K}^{-1}$  can be achieved by growing HEMTs over GaN bulk substrate.

As mentioned in Figure 14 600 V GaN EMT has been introduced in market by many suppliers. Transphorm has demonstrated the applicability of GaN HEMTs in realization true bridgeless Totem Pole PFC. This circuit will be discussed in detailed in later chapters. Transphorm presented in 2014, that 99% efficiency can be achieved by employing GaN HEMTs in totem Pole PFC circuit. Another application that they developed is “All in one Power supply” in which they used GaN HEMTs in bridged PFC circuit and LC resonant converter to achieve efficiency of greater than 90%. We will discuss both these application in detail with practical results in later chapters. It has also been revealed in ISICPEAW 2015 that GaN HEMTs with 1200V rated voltage has also been developed. However they are not yet ready to be released commercially.

### 2.3.3 Gate Injection Transistors:

Heterojunction AlGaIn/GaN devices suffer from low gate threshold voltage which leads to higher leakage current. Gate Injection transistor is inheritably normally off device with very high drain current carrying capability got introduced in (Uemoto, Hikita et al. 2007).

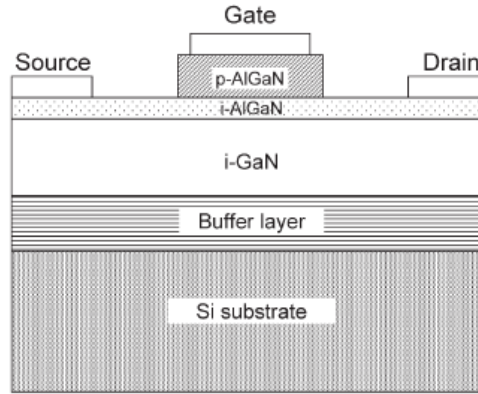


Figure 16: AlGaN/GaN Gate Injection Transistor (GIT)(Uemoto, Hikita et al. 2007)

The main feature of this structure is p doped AlGaN over the heterojunction of AlGaN/GaN (Uemoto, Hikita et al. 2007). P-doped AlGaN deplete the channel, and hence realize the normally off operation of GIT.

Under zero biasing voltage, no drain current will flow. As gate to source voltage will increase, drain current will start increasing and GIT will act as a standard FET. However, as the gate voltage increase exceeding the forward built-in voltage  $V_F$  of P-N junction, gate will inject holes in to the channel (Uemoto, Hikita et al. 2007). This transistor got its name because of this property of injecting holes in to the channel.

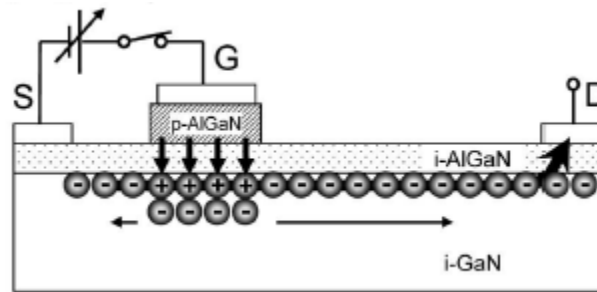


Figure 17: Gate Injection Phenomena of GIT (Uemoto, Hikita et al. 2007)

In order to maintain the charge equilibrium in channel, equal number of electrons will accumulate under the holes discharged by gate into channel. Drain to source potential will sweep away these electrons, while holes will stay around the gate as holes mobility is almost two times slower than that of electrons. This phenomena results in massive increase in drain current with low gate current.

Fabricated GITs showed excellent on and off characteristics. For gate threshold voltage of 1 V, high drain current of 200 mA/mm was achieved with low specific ON



resistance of  $2.6 \text{ m}\Omega\text{cm}^2$ . This technology is still immature with a lot of room for improvement.

In order to test the performance of GIT, Inverter for Motor Drive based on GITs was implemented by (Ishida, Ueda et al. 2013).

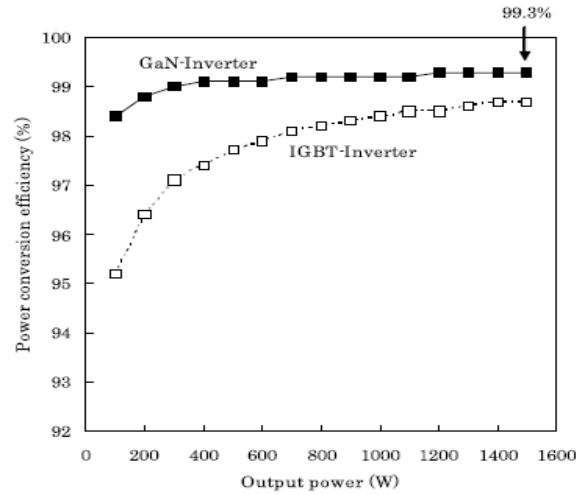


Figure 18: Inverter Efficiency comparison (Ishida, Ueda et al. 2013)

## 2.4 Reliability Issues:

SiC and GaN devices are still on the rail of development. Newer technologies results in thinner oxide layer and greater electric fields which makes the reliability of devices very challenging. SiC and GaN devices are known for high switching and low power loss switches. However due to structural limitation of GaN device the maximum break down voltage observed is 1000V, but switching frequencies can be as high as 500 kHz, which makes GaN devices ideal for low voltage high frequency applications. While SiC devices take hold of high power devices, as they have higher break down voltage.

In GaN devices the main cause of failure is electron trapping in the oxide layer. As when high voltage is applied, the electrons will trap in the oxide layer. These electrons will heat up and will collide with crystal to generate more hot electrons and eventually will end up in breakdown of oxide layer. The most important technical defect that is being observed is Current Collapse phenomena in GaN transistors. Basically in current collapse phenomena, the drain resistance increases after OFF-state stress is being applied across the drain and it results in collapsing of drain current to low value.

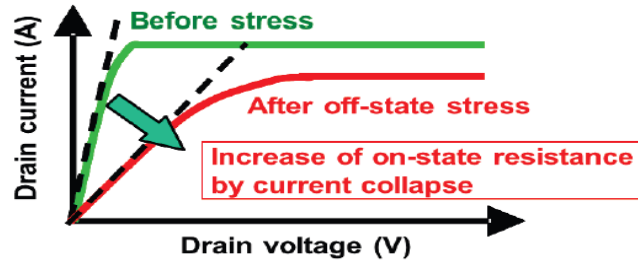


Figure 19: Current Collapse Phenomena (Ueda 2014)

However by certain means we can avoid this current collapsing and phenomena and commercialization of GaN transistors has already been started, they are being used in cellular base stations for low voltages of 50V (Ueda 2014).

In GaN devices, normally OFF transistors has always been a challenge. But GaN Gate Injection Transistors (GIT) have almost solved this problem as well. The most notable characteristics of these transistors is their very low  $R_{ON}Q_g$  product value ( $R_{ON}$ : on-state resistance,  $Q_g$ : Gate Charge). According to estimate this product value ( $R_{ON}Q_g$ ) of GIT is almost thirteen times lesser than that of normal Si MOSFETs, which depicts almost ideal behavior of GaN GIT for fast switching (Ueda 2014). It's been also observed that these GIT are also free from Current Collapse phenomena. Drain voltage was increased till 600V but these GITs did not show any sign of drain current collapse.

Stability of leakage current and threshold voltage over 1000 hours indicates that this device maturity is progressing at good pace.

SiC based Double Diffused MOSFET (DMOS) act as potential replacement of Si MOSFETs. One main issue that is being faced during the operation of DMOS is shifting Gate biasing Threshold voltage. Reason behind this is the trapping of electrons or holes in the oxide layer.

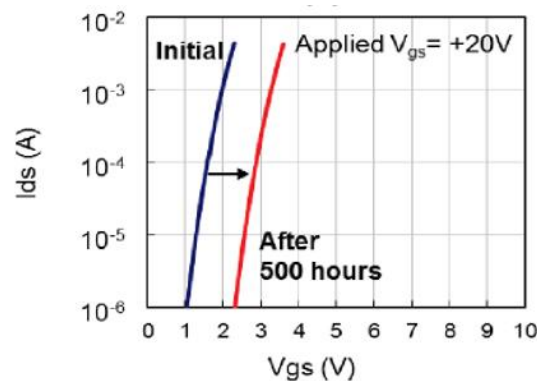


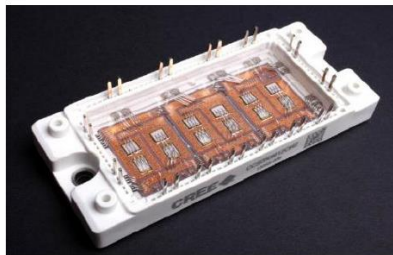
Figure 20: Shifting of Gate biasing Threshold voltage (Ueda 2014)

DMOS also suffers with degradation of body diode. Main reason behind this is basal plan formation. These problems call for improvements in epitaxial layer. For applications where reverse drain to source current flow is required like in converters for motors, an additional fast recovery SiC based Schottky diode is added in to the package of DMOs. This certainly has almost doubled the cost of DMOS but it provides a good solution to body diode degradation problem.

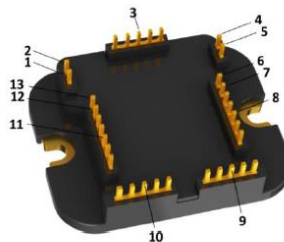
As in DioMOS, forward current will not flow through the P-N junction, hence this device is free from body diode degradation. No change in gate bias voltage, stable threshold voltage and minimal drain leakage current depicts that DioMOS is reliable enough to be used in practical applications.

## 2.5 [Packaging Technologies for WBG Semiconductor Devices:](#)

With introduction of wide band gap devices in high power ultra-fast applications, with operating temperature of around 300 °C, new techniques of packaging are required to take full advantage of their superior properties. Requirements of packaging include Ultra low parasitic inductance, High current density, Lower losses, higher package E-field stress and to withstand environmental stresses. At higher switching speeds parasitic inductances become more critical. There has been few advancements in packaging of SiC devices. A few examples of commercially available packaging of SiC devices are shown in Figure 21 & Figure 22:



*Figure 21: SiC 1200 V six pack power Module*



*Figure 22: 1200 V SiC Full Bridge*

Figure 22 SiC full bridge can operate at high temperatures around 225 °C.

STmicrocontrollers have reached major bench mark in SiC technology. They have fabricated plastic casing for SiC MOSFETs with rated voltage of 1200 V and it has a capability to operate at ambient temperature of 200 °C.



*Figure 23: Plastic Casing MOSFET by STmicrocontrollers (Bindra 2015)*

One very big project with the name of compact, smart and reliable drive unit for fully electric vehicles (COSIVU) under FP7 is aiming to develop smart unit for electrical vehicles. Aim of their project is to develop packaging of SiC device with better thermal conductivity, so that device area can be further reduced to increase the power density. They have introduced double sided cooling of power devices to have better cooling and hence will have better thermal conductivity.

SiC power devices are available commercially in the form of discrete devices as well as power modules. However, GaN power devices are yet to get matured. GaN HEMTs are only available in discrete form up till the range of 600 V.

## 2.6 Application of WBG Devices:

Superior qualities of wide band gap devices have been discussed in detail in previous sections. We have continuously been discussing there applications as well. However in this section we will briefly review the major breakthroughs achieved in three major applications of WBG power devices.

In Figure 24 applications of Si, SiC and GaN are segregated on the basis of switching frequency and operating voltage. As SiC devices have high gate threshold voltage and higher turn ON and OFF times as compared to GaN devices so they are considered ideal devices for high voltage and medium range frequency applications. However, GaN devices are used for low power but very high switching frequency application because of low gate capacitance.

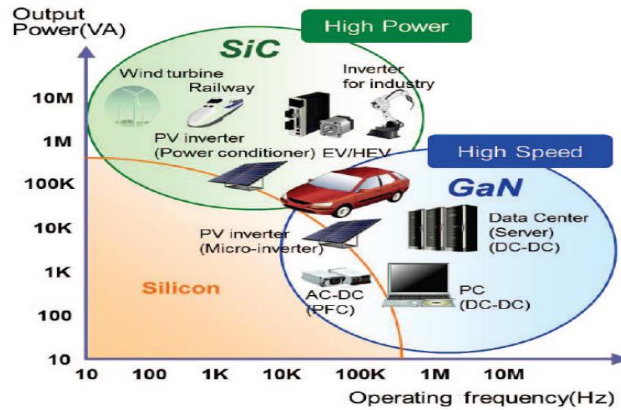


Figure 24: Applications of WBG devices (Ueda 2014)

Figure 25 shows the market forecast of WBG power devices. It is pretty much obvious that SiC power devices are way more mature than GaN power devices. However, it has been predicted by many experts that because of breakthroughs obtained by GaN devices especially in the field of PFC circuits, GaN devices will surpass SiC power devices in a decade or so.

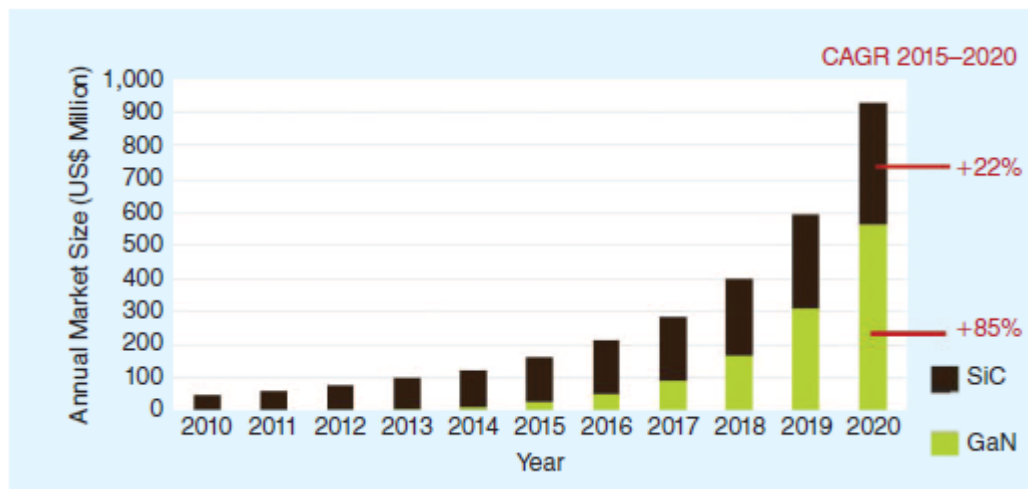


Figure 25: Market forecast of WBG power Devices (Bindra 2015)

### 2.6.1 Traction Systems

Higher break down strength of SiC, makes it attractive choice of high voltage applications like rail systems. Rail application like train tractions voltage is expected to go in kV (>17kV). It is expected that these applications will soon adopt these WBG power devices especially SiC devices. Experts at Yole believe that these high voltage applications are exactly the place where SiC power devices should be. According to them it is being estimated that during the time frame of 2018-2020, applications related to train systems will expand at the rate of 50% per-annum.

Keeping in view these prospects of SiC, many companies related to train transportation are investing in different projects. In electrical vehicles ON board current weight carrying capability and space is usually limited. Keeping in view these constraints, BOMBARDIER a Swedish train company is working on compact 1000KVA converter module for their electric trains based completely on SiC MOSFETs.

Comprehensive study on application of SiC Power devices in Rail traction system is being studied in (Fei Shang, Arribas et al. 2014). 40kW inverter with SPWM was implemented to characterize the behavior of different switches and diodes. All per unit percentages for different combinations in Figure 26 were calculated with respect to losses in Si IGBT and Si diode.

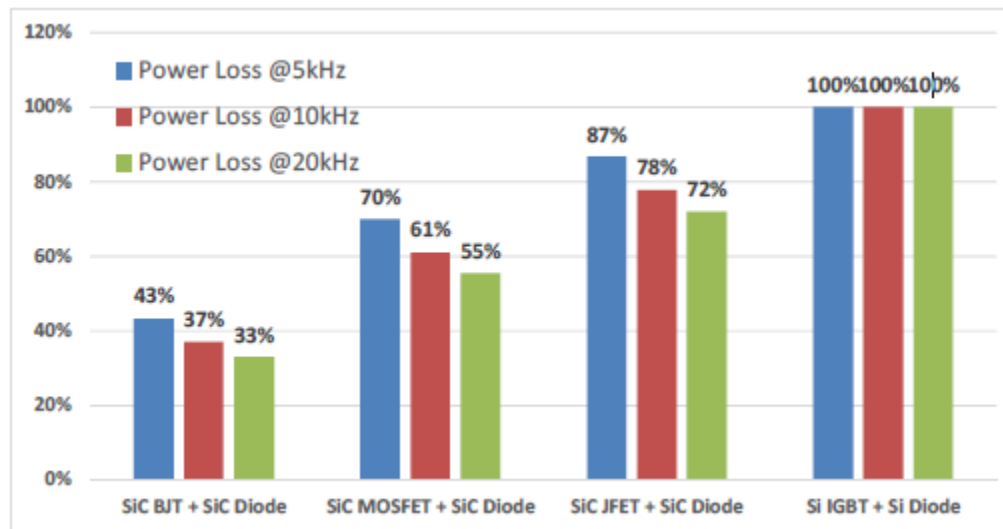


Figure 26: Power Loss Comparison of SiC and Si Devices (Fei Shang, Arribas et al. 2014)

To reduce the area of inverter, Mitsubishi announced in 2013, to develop their Railcar Traction inverter completely based on SiC power devices. 3.3 kV/1.5kA inverter was developed with SiC MOSFETs and SiC diodes. 55% reduction in switching losses, 30% reduction in total consumption of electricity of railcar systems was being observed after replacing conventional Si IGBTs with SiC MOSFETs (MITSUBISHI ELECTRIC 2013).



Figure 27: Area comparison between SiC and Si Inverter (MITSUBISHI ELECTRIC 2013)

### 2.6.2 Power Supplies

GaN is very promising device for switch mode power supplies. Generally switching frequency of power supplies is limited to few hundreds of kHz. If we can increase this switching frequency to MHz range then we can reduce the switching losses, increase the power density and reduce the losses and size of magnetic components including inductors, capacitors and transformers.

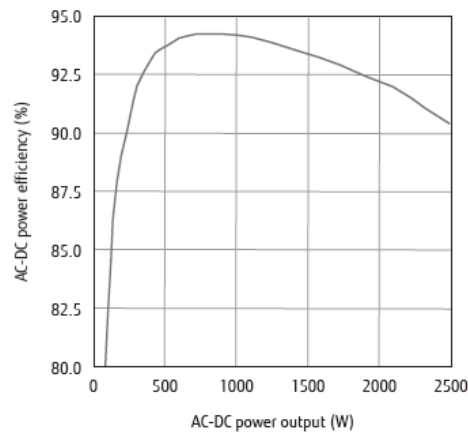


Figure 28: GaN HEMT based Power System Efficiency Graph (Joshin, Kikkawa et al. 2014)

Even though GaN devices are still in development phase, GaN based power supplies generated the revenue of 10-12 Million USD (Bindra 2015). It is being estimated in Yole's "Power GaN Market and SiC Modules, Devices, and Substrates for Power Electronics Market" that market of GaN Power devices will reach 550 million USD level till 2020. 600 V GaN HEMT on Si substrate has opened a new era in Power electronics applications. It is estimated that GaN HEMT will take over the Power factor Correction circuit sector with in few years.

All-In-One power supply by Transphorm is completely based on GaN HEMT. We have one prototype of that power supply and we will discuss it in detail in later chapters.

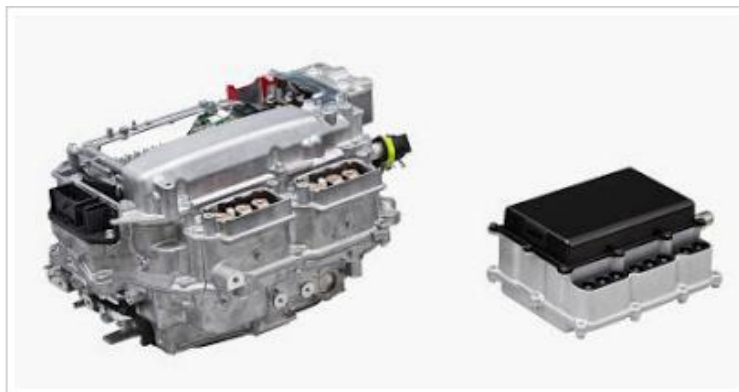
### 2.6.3 Electrical Vehicles

Electric vehicles is another high voltage application for SiC devices. The major problem of acceptance of Sic power devices for EV has been their cost effectiveness and reliability. However with production of improved quality wafers by many supplier it is being believed by experts at Yole that 2018 will be the year of acceptance of SiC power devices to be accepted by Electrical vehicles. It is being estimated that SiC power devices will generate revenue of 25 Million USD by 2020 with acceptance of SiC based converters in electrical vehicles (Bindra 2015).

Shinry Technologies is a China based company that specializes in production of DC-Dc converter, on-board charger and rapid charger solutions for Electric Vehicles. It has

been reported that after employing SiC MOSFETs from CREE, they have achieved 25% reduction in their product size and 60% reduction in overall losses as compared to their conventional Si based converters (CREE 2013).

Power Control Unit (PCU) plays an important role in hybrid or electrical vehicle (EV). PCU is considered as the brain of electrical vehicle. PCU is responsible for control and proper functionality of electronic inverters. Almost 25% of all losses in EV are contributed from PCU and 20% of losses of PCU comes from power semiconductors alone. So Toyota in 2013, employed SiC power devices in their PCU and improved the overall efficiency by 10% and reduced the size by 80% as compared to their Si based PCU (Electric Vehicle News 2014).



*Figure 29: Size Comparison of Si and SiC PCU by Toyota (Electric Vehicle News 2014)*



## Chapter 3. Power Factor Correction (PFC) Circuits:

### 3.1 Origin of Power Line Distortion:

Emerging applications of Power electronic devices have raised many questions on Power Quality, which has become one of the hot topics among researchers. Power Quality can be defined as the extent to which actual voltage and current waveform corresponds to sinusoidal waveform (Singh, Singh 2010).

Power Electronics devices especially Variable frequency drives (VFDs), Switch Mode Power supplies (SMPS) etc. are widely used in industrial and domestic applications. These devices draw discontinuous current in the form of pulses from the source and hence become the major contributor of harmonics in Power system. Harmonics can be defined as the components of voltage or current with frequencies that are integral multiples of fundamental frequency (Singh, Singh 2010).

#### 3.1.1 Power Factor:

Power Factor is the ratio of actual power delivered to load (Real Power) to the product of root mean square (RMS) value of voltage and current (Apparent Power) (Emanuel 1993).

$$Pf = \frac{P}{S} \quad (3-1)$$

Where  $P$  is real power and  $S$  represents apparent power.

In case if current waveform is pure sinusoidal, than power factor can be defined as the cosine of angle between voltage and current waveform (Fairchild 2004). Depending upon the type of load, power factor can either be inductive or capacitive. When current and voltage will be in phase then power factor will have maximum value of 1. All exercise of power factor correction is being done in order to make power factor as close as possible to 1.

$$Pf = \cos\phi \quad (3-2)$$

$\phi$  is displacement angle between voltage and current. This definition is only true if current waveform is pure sinusoidal. It can also be termed as displacement power factor.

However, definition of power factor changes with introduction of harmonics in current signal. In that case, product of displacement factor and ratio of fundamental

component of current to its RMS value defines the power factor of system (Mohan 2003).

$$Pf = \frac{I_1}{I_{RMS}} * \cos\phi \quad (3-3)$$

$I_1$  is first harmonic of current,  $I_{RMS}$  represents RMS value of current.

Harmonics generated by power electronic devices have adverse effect on Power Factor of the system. An ideal power factor means that both voltage and current should be sinusoidal. However, in actual systems with SWMPS, VFDs etc. current waveform becomes non-sinusoidal and hence lowers the power factor. Low power factor means lesser active power being transferred to the load (Grigore 2001).

### 3.1.2 Effects of Harmonics on Power System:

As mentioned above, harmonics generated by Power electronic devices are very harmful for power system's quality. A few of the effects include (Grigore 2001):

- Increased losses in cables, transformers, capacitors and other power system equipment.
- Overheating of equipment.
- Cause pre-mature aging and failure of equipment.
- Damages insulation of transformers and capacitors.
- High frequency harmonics cause interference with telephone cables and increase audio noise.
- Oscillation in electrical machines.

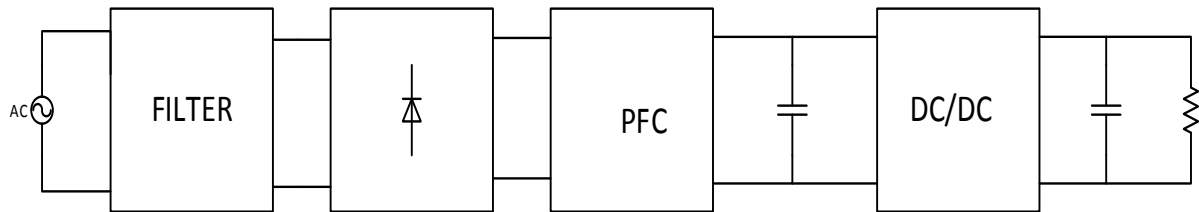
### 3.1.3 Standards for Line Current Harmonics Regulation:

Higher switching frequencies of semiconductor switches to achieve higher efficiency and power density results in higher dv/dt and di/dt that will increase the interference noise in utility line (Redl 1996). Negative effects of power electronic devices on the power system, urged the requirement of regulation of noise and put limits on harmonic content. Limits are more critical for high power devices. More detailed information about limits imposed by different standards can be found in (Grigore 2001) and (Redl 1996).

### 3.2 Introduction to PFC Circuits:

To reduce line harmonic pollution and to keep the power quality in acceptable range, Power factor correction is required. Power factor correction devices have been developed and researched quite extensively (Chen, Dai 2013). Ideally speaking, PFC circuit should make the whole circuit behave like an ideal resistor while maintain the voltage regulation. As input voltage is normally sinusoidal, so PFC device would be a driving force or control circuit that will force the line current to follow sinusoidal path (Grigore 2001).

In order to supply smooth DC input while maintaining power factor close to unity, PFC circuits are employed at the input of DC/DC converter. One very common application of PFC circuits, is DC power Supply.



*Figure 30: Power Supply Block Diagram*

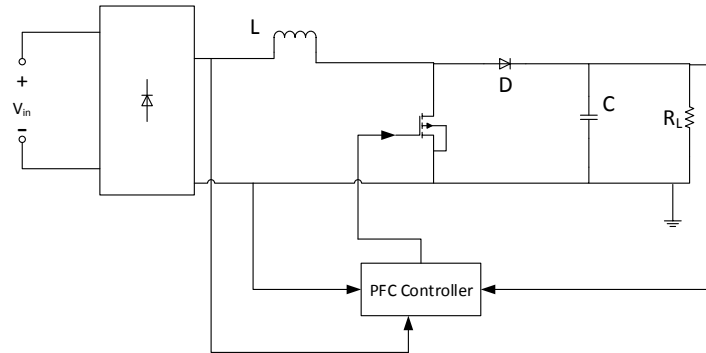
DC power supplies are used both in domestic and industrial appliances. In order to meet the strict Electromagnetic interference standards, PFC circuit along with filter at its input, insure approximate sinusoidal current along with electrical noise within permissible range (Mühlethaler, Uemura et al. 2012).

There are various methods of Power factor correction including active and passive techniques. Detailed analysis of all these techniques can be found in (Grigore 2001). We will restrict our discussion to active power factor correction circuits by employing boost converter. In next section we will discuss about control of PFC circuit, however significance of Boost converter will be discussed in later sections.

#### 3.2.1 Basic Principle:

As described in previous sections, basic function of PFC circuit is to force the mains current to follow sinusoidal path. Without PFC circuit, converters usually have power factor around 0.6 and hence considerable amount of harmonics will be injected in to power system (Fairchild 2004).

PFC circuit includes a diode bridge rectifier followed by a Boost Converter. Block diagram of Basic PFC Circuit is given below:



*Figure 31: Basic Boost PFC*

Normally input of Boost converter is smooth rectified DC voltage. To eliminate the ripple from input rectified voltage, a bulk capacitor is installed at the input of converter. However in PFC, Boost inductor current has always to be proportional to the line voltage. Power Factor Control circuit requires the input voltage signal for shaping the Boost Inductor current. That is why PFC circuit does not employ input bulk capacitor. Hence, the input voltage ranges from zero to peak input value with twice the frequency of AC mains supply (Fairchild 2004). All feedback signals to PFC Controller including input voltage feedback signal will be discussed in later sections.

Gate driving signal from PFC controller, drives the switch in such a way that Boost inductor current follows the reference signal. Output Bulk capacitor absorbs the pulsating current and hence smooth DC current will flow through the load (Rossetto 1994).

### 3.3 PFC Control Techniques:

There are various control techniques that can be used in PFC Circuits. These control techniques include:

- Peak Current Control.
- Average Current Control.
- Hysteresis Control.
- Borderline Control.

As scope of this thesis is only limited to Peak Current Control and average current Control, so we will not discuss the rest of the techniques in detail. Detailed description of all PFC control techniques can be found in (Rossetto 1994).

### 3.3.1 Peak Current Control:

Fundamental circuit for peak current control is:

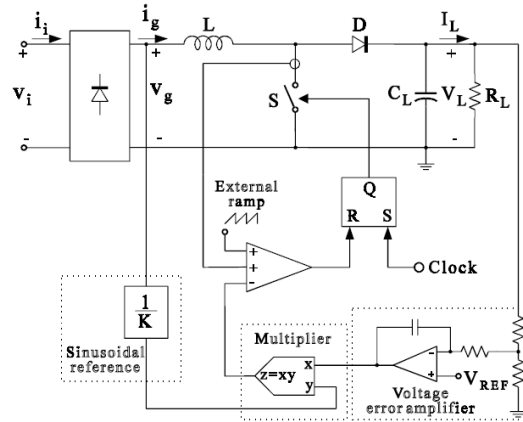


Figure 32: Fundamental Circuit for Peak Control PFC (Rossetto 1994)

Sinusoidal reference, is basically the rectified input AC voltage. Switch will be turned ON with constant frequency that will be decided by the external clock. Switch will be turned OFF as soon as the sum of inductor current and external ramp (purpose of external ramp under next heading) will reach the level of output of voltage multiplier. Input to this voltage multiplier includes error voltage signal and scaled sinusoidal reference (Redl, Balogh 1992).

Apart from shaping the inductor current, another function of PFC control circuit is to regulate the output voltage. Voltage error amplifier generates the error signal, and value of that error signal depends upon the deviation of scaled output voltage from reference voltage  $V_{REF}$ . Value of scaled output voltage depends upon the resistor value in divider. As soon as the scaled output voltage reaches the level of  $V_{REF}$ , value of error signal will become almost zero resulting in switching OFF the switch.



Figure 33: Peak Current Control Proposition (Rossetto 1994)

Duty cycle of the power switch depends upon the input reference voltage. As the input sinusoidal reference varies from zero to maximum value, duty cycle varies from its maximum value to its minimum value. (Zhou, Jovanovic 1992).

### 3.3.2 Stability Issues in Current Controlled Converters:

External ramp function is used in PFC circuit, in order to make current controlled Boost converter stable over all ranges of duty cycle for constant frequency operation.

It's been known for many years that fixed frequency operated current mode controlled converters, have stability issues for duty cycles over 50% (Redl, Novak 1981). Instability conditions are observed for inner current loop, however voltage current loop shows stability over entire range of duty cycle. There are many converters which when operated at fixed frequencies, cannot go beyond duty ratio of 50%. This instability issue, makes current controlled converters unsuitable for many applications, especially, for the applications with variable input voltage (Unitrode 1999).

Graphically this instability issue can be described as:

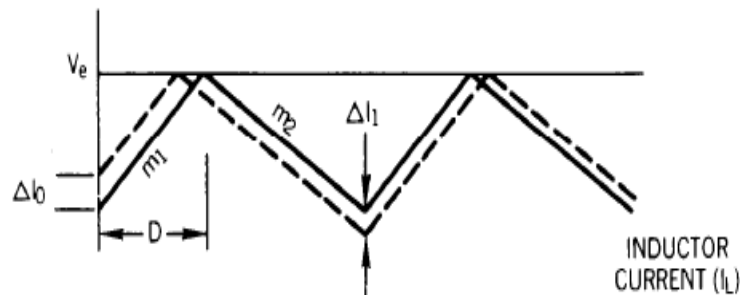


Figure 34: Inductor Current: Duty cycle < 50% (Unitrode 1999)

Above figure shows the inductive current for Current Controlled converter controlled by constant reference voltage  $V_e$  signal. It can be seen that for duty cycles less than 50%, for a change in inductor current of  $\Delta i_0$ , the error in current signal decreases with time. This ensures the stable operation of converter for duty cycles lesser than 50%.

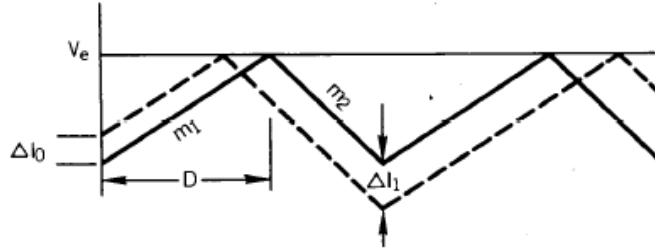


Figure 35: Inductor Current: Duty cycle > 50% (Unitrode 1999)

However for duty cycles greater than 50%, the error in inductor current signal keeps on increasing with time, and hence makes the converter unstable.

One solution of this problem is introduction of artificial slop along with inductor current in current loop (Redl, Novak 1981). This method is known as slope compensation method. It's been observed that introduction of slope in inner loop, results in stability of control loop for all values of duty cycle (Unitrode 1999).

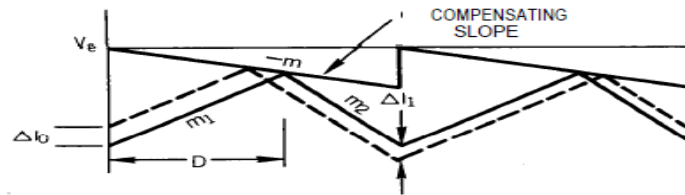


Figure 36: Inductor Current: Duty cycle > 50% with Slope Compensation (Unitrode 1999)

Compensating slope function either can be added to inductor current signal or subtracted from voltage reference signal (Unitrode 1999).

However, this compensation can be avoided by keeping the duty ratio less than 50%, but in that case PFC circuit will only be used for specific applications with constant input voltage (Rossetto 1994).

### 3.3.3 Average Current Control:

Introduction of current error amplifier in control circuitry, will give better shaping of inductor current. Average current controller takes the average of inductor current and then compares it with fixed ramp function to generate the appropriate gate signal for the switch. (Zhou, Jovanovic 1992).

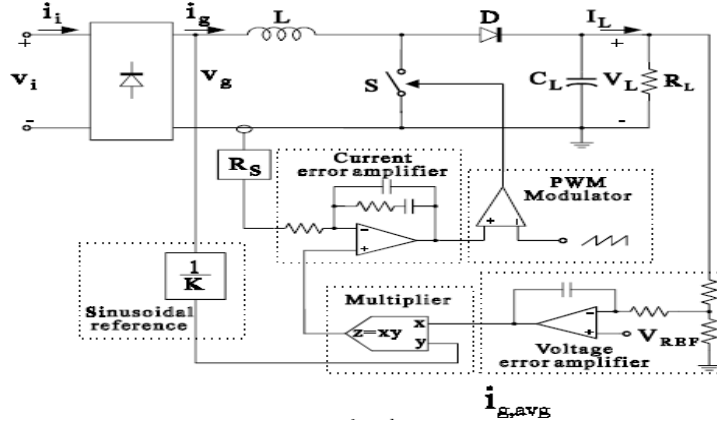


Figure 37: Average Current control Schematics (Rossetto 1994)

Rest of the control circuitry is similar to that explained in section 3.3.1.

This method of PFC control is becoming very popular nowadays and its detailed design procedure can be found in (Zhou, Jovanovic 1992) & (Redl, Balogh 1992).

#### 3.3.4 Error Amplifier:

Regulated DC/DC converters have wide range of applications. Most of the times input voltage is variable, while DC output voltage should be kept regulated at certain desired level. This can be achieved either by varying the ON time of Power Switch or by varying the switching frequency. Usually variable duty cycle method is used for regulating the output voltage, as variable switching frequency makes it difficult to filter the high frequency components in both output and input voltages and currents of converter (Mohan 2003).

In PFC control circuit, Figure 8, PWM modulator is being fed by output of current error amplifier. Voltage error amplifier serves as the input to Current amplifier. Both current error amplifier and voltage error amplifier are comparing the inductor current and output voltage respectively with fixed reference value. As described above, error signal will control the PWM modulator to regulate the output voltage.

##### 3.3.4.1 Characteristics of Feedback Compensator:

As described above, PFC control circuit has two feedback compensation loops i.e. Voltage error Amplifier and Current error Amplifier. Following characteristics are desired from feedback loops for stable operation (Musavi, Edington et al. 2013) & (Mohan 2003):

- The gain of compensation loop should be high at low frequencies, to minimize the steady state error.



- Gain should be low for frequencies around switching frequency and higher, in order to reduce the effect of high frequency switching transients on output.
- To ensure the stable operation, phase margin should be in the range of 45° to 60°.

Error amplifier that is being used in our control circuit is known as type 2 amplifier. This type of compensator is referred as type 2 amplifier because of existence of two poles in its transfer function (Venable 1986).

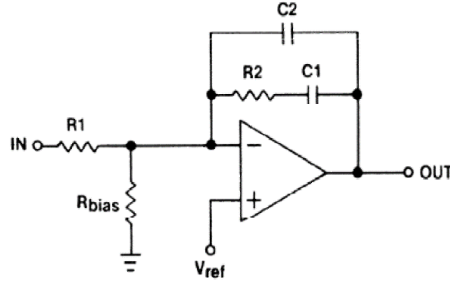


Figure 38: Type 2 Amplifier (Mohan 2003)

Transfer function of Type 2 amplifier can be given as (Mohan 2003):

$$T_c(s) = \frac{1}{R_1 C_2} \frac{s + w_z}{s(s + w_p)} \quad (3-4)$$

As mentioned above, type 2 amplifier has two poles and one zero. Single 's' in the denominator of equation (3-4) shows the presence of pole at origin. To stabilize the system and control the phase margin a zero and pole pair is introduced (Venable 1986).

$$w_z = \frac{1}{R_2 C_1} \quad (3-5)$$

$$w_p = \frac{C_1 + C_2}{R_2 C_1 C_2} \quad (3-6)$$

Position of poles and zeros defines the stability of system. There are many methods to find the position of zeros and poles that will ensure the stable operation of particular system. We will not go in to the details of calculations. However, detailed calculation and explanation can be found in (Mohan 2003). Design equations are being derived on the basis of poles and zeros location. Design equations for type 2 amplifier includes (Mohan 2003):

$$C_2 = \frac{G_1}{KR_1w_{cross}} \quad (3-7)$$

$$C_1 = C_2(K^2 - 1) \quad (3-8)$$

$$R_2 = \frac{K}{C_1w_{cross}} \quad (3-9)$$

$W_{cross}$  is cross over frequency and it can defined as the frequency at which gain of compensator will become 0dB or 1 (Venable 1986).

$R_1$  is chosen randomly and that value is used to calculate the rest of the parameters. Value of 'K' is calculated by K-factor approach for stability analysis of control systems.

### 3.4 Modes of Operation:

There are two modes of PFC, based on the flow of current through Boost Inductor.

- Continuous Conduction Mode (CCM)
- Dis-continuous Conduction Mode (DCM)

In Continues conduction operating mode (CCM), the Boost Inductor current never reaches to zero (Grigore 2001). During ON time of switch, the Boost Inductor is charged and discharged during the OFF time period. In CCM Boost inductor never discharges completely. High power PFC circuits operate in CCM.

In discontinues conduction mode, inductor discharges completely during the turning OFF time of the switch. Due to intrinsic behavior of Boost Converter, in DCM inductor current approximates to sinusoidal waveform and it can be used as PFC circuit without any external control.

Inductance value of Boost Inductor ensures the operation of Boost converter in desirable region. Equation for Boost inductance can be given as (Mohan 2003) :

$$L = \frac{T_s V_o}{2I_{LB}} D(1 - D) \quad (3-10)$$

Here,  $T_s$  is switching time period,  $V_o$  is output voltage,  $D$  is duty cycle ratio and  $I_{LB}$  is average inductor current.

Inductance value obtained from above equation will ensure the operation of converter on boundary between continuous and discontinuous mode. Large inductor will make the converter to operate in continuous conduction range and vice versa.

Due to large current swings in discontinuous conduction mode, converter operating in DCM will have greater  $I^2R$  losses. Core of Inductor used DCM mode is bigger than that used in CCM and hence will become inefficient for higher current. Large current swings will cause higher electrical noise and hence requirement of filter will be increased. Because of all these reasons DCM operated PFC circuits are normally used for applications lesser than 300W (Fairchild 2004).

### 3.5 Different Topologies of PFC Circuit:

As mentioned earlier, Boost converter is employed as PFC circuit. With increasing demands of high performance converter, there have been a number of modifications in conventional boost converter PFC. In this section we will discuss working principle, merits and demerits of different PFC circuit topologies.

#### 3.5.1 Conventional Bridged Boost PFC:

Boost topology has always been an excellent choice as a Power factor correction circuit. Boost topology has many advantages over other converter topologies. These advantages include (Yang, Jiang et al. 1993):

- Mains current can be controlled directly by controlling the Boost inductor current.
- Ripple in input current can be controlled by carefully designing the boost inductor.
- Low voltage stress on the switch.

Circuit diagram of Conventional Boost PFC:

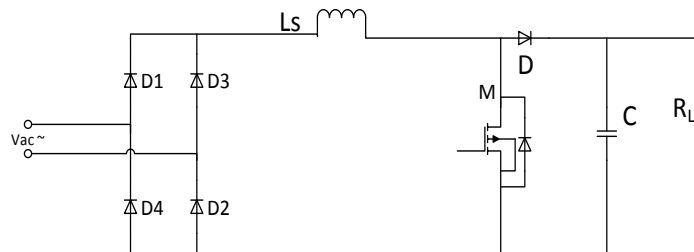


Figure 39: Conventional Boost PFC (GaN 2013)

Conventional PFC circuit incorporates diode full bridge to convert AC input voltage in to DC. After that there is Boost section which will step up the voltage. Hence output

Dc voltage will always be greater than maximum input voltage (Ancuti, Svoboda et al. 2014).

Losses across the semiconductor devices contribute a major portion in overall losses of converter. In conventional Boost converter, there are 3 semiconductor devices conducting during each cycle, i.e. D1, D2, M when MOSFET is conducting and D3, D4 and D when MOSFET is in OFF state.

Diode D is usually high frequency SiC Schottky diode with minimal forward voltage drop. However, diode bridge has line frequency silicon diodes with forward drop of around 700mV. In conventional PFC circuit, there are two bridge diodes conducting all the time, and this is continuous source of inefficiency in circuit.

Loss distribution of 500W conventional Boost PFC circuit revealed that the major contributor of losses in converter is diode Bridge (GaN 2013). Existence of input bridge puts a limit on efficiency of converter (Chen, Dai 2013), so if we eliminate input bridge and incorporate it in Boost converter circuit, we can avoid major portion of losses. The next topology that we will discuss utilizes this approach to achieve major breakthrough in realization of efficient converter.

### 3.5.2 Bridgeless PFC Topology:

Bridgeless PFC topology, as its name implies is novel topology which eliminates the requirement of input bridge and incorporate it into Boost Circuit (GaN 2013).

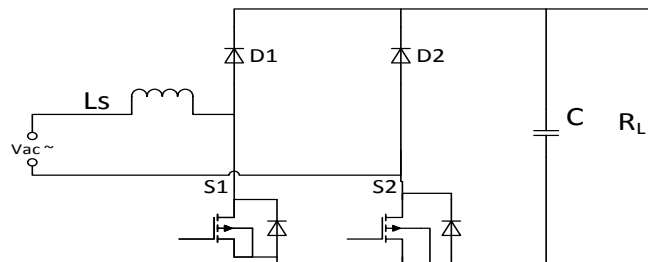


Figure 40: Bridgeless PFC Topology (Li, Andersen et al. 2009)

As explained before, with increasing power demand and heating losses, bridged PFC becomes very inefficient. Its operation can be explained as (Rajappan, John 2013):

- During positive input AC cycle, gate of switch S1 is driven high. Hence current will flow through S1 and will return through the body diode of S2. This will be the charging cycle of inductor  $L_s$ .
- To discharge the inductor and to transfer energy to load, S1 is turned OFF and current will flow through diode D1 and will return through body diode of S2.

- When AC input voltage gets negative, S2 is driven high to charge the inductor. Now body diode of Switch S1 will provide the return path to current.
- As soon as S2 is turned OFF, the current will flow through D2, transfer energy from source to load and return through body diode of S1.

Both bridgeless and conventional bridged PFC circuit operate as Boost converter. Though, bridgeless PFC has two switches but only one switch operate at a time and the other switch provides a return path to current through its body diode. Hence, the switching losses for both converters are same. However, bridgeless PFC circuit cuts down the conduction losses. In conventional PFC circuit, there were three semiconductor devices conducting each cycle, however in bridgeless circuit only two semiconductor devices conduct every cycle. Two low frequency diodes of Diode Bridge are being replaced with two MOSFETs, providing the return path to current. So difference in conduction losses of both converters depends upon the difference between forward voltage drop of low frequency diodes and body diodes of MOSFETs.

As explained in previous section, inductor current of PFC circuit needs to be sensed to control the switching pattern. In bridgeless circuit, a complex sensing circuit will be required. Moreover high frequency switching of body diodes of switches makes it difficult to operate the converter in CCM (Chen, Dai 2013).

In conventional bridged PFC circuit, ground of AC source is always connected to load ground through input diode bridge. In bridgeless PFC circuit, AC source ground is connected to load ground during positive half cycle through the body diode of S2, but during negative cycle of input voltage, AC source ground is connected to negative terminal of load through switch S2 during charging of inductor output and connects to positive terminal of load during the discharge of inductor. Hence source ground keeps on pulsating with respect to load and leads to common mode noise (Huber, Jang et al. 2008).

To reduce the common mode noise generated by Bridgeless PFC, another circuit was being proposed (Rajappan, John 2013).

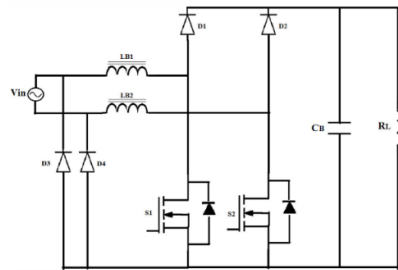


Figure 41: Bridgeless PFC Circuit-CM Noise Reduction (Rajappan, John 2013)

Diodes D3 and D4 are added to provide a low frequency path between input source and load terminals. Two inductors are used in this circuit, one for each half cycle. Detailed operation and analysis of this circuit can be found in (Rajappan, John 2013).

### 3.5.3 Totem Pole PFC:

Totem Pole PFC circuit is modification of simple Bridgeless PFC, which is obtained by swapping switch S2 with diode D1. This circuit got its name because of the positions of switches S1 and S2.

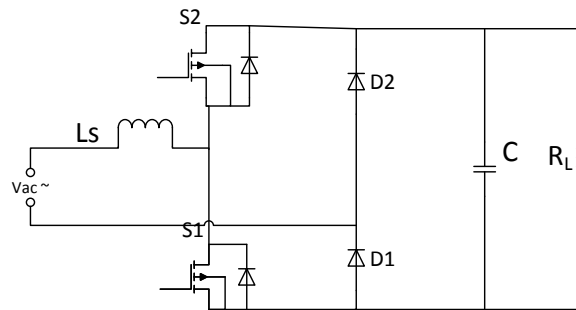


Figure 42: Totem Pole PFC Circuit (Chen, Dai 2013)

Operation of this circuit can be explained as:

- During the positive cycle of supply voltage, to charge inductor  $L_s$ , gate voltage of switch S1 is turned high and diode D1 provides the return path to current.
- Once the inductor is charged to specified level, S1 is turned OFF and S2 is turned ON to transfer the energy from supply to load.
- During negative half cycle, inductor is charged through S2 and discharged through S1.

Both switches S1 and S2 are operated complementarily. Like basic bridgeless PFC circuit, totem pole circuit also has two semiconductor devices conducting during each half cycle, which makes it more efficient than conventional bridged PFC circuit. In totem pole PFC circuit, diodes D1 and D2 always connects the source ground to load ground and hence solves the problem of common mode noise generation in basic bridgeless PFC circuit. Another advantage of this circuit over circuit in Figure 41 is lesser number of devices. In Figure 41 two diodes D3 and D4 are added to solve the common mode noise problem, however in totem pole PFC circuit, this issue got resolved without any addition of extra diodes.

Merits of this topology can be summarized as (GaN 2013):

- Lowest component count as compared to other PFC topologies.

- Potential of reaching very high efficiencies.
- It does not generate large common mode noise.

Despite of all these merits, Totem pole PFC circuit could not find many applications because of characteristics of conventional switches. For conventional Silicon MOSFETs reverse recovery time of their body diodes is usually longer than that of fast-recovery Schottky diodes. Slow reverse-recovery characteristics of body diodes makes it impractical to use this converter in CCM (GaN 2013). Usually totem pole PFC converter is used in DCM or at boundary between CCM and DCM i.e. CRM. Otherwise in CCM mode of operation reverse recovery losses will become significant and will put a limit over efficiency of converter (Chen, Dai 2013). This converter can be used in Zero-Voltage-Switching mode to overcome switching losses and to reduce the stress on switches and diodes. But then again it will put a limit on power range of converter (GaN 2013).

As mentioned in previous sections, high power PFC converters become inefficient when operated in DCM or CRM mode. However this problem with Totem Pole PFC can be resolved by introducing WBG switches. In next section we will discuss that how WBG switches can make Totem Pole PFC to reach immense heights of efficiency

### 3.6 WBG in PFC:

Introduction of Wide band gap devices has brought a new revolution in Power Electronics industry. Extremely low switching losses, bidirectional flow of current and approximately no reverse recovery current makes these devices ideal choice for highly efficient PFC circuits.

Power Factor correction circuit is essential part for every power supply and this technology of WBG devices has provided us with new solution for prevailing power supply issues. For last decade, tremendous effort has been done in order to improve the efficiency of PFC, and hence improving the efficiency of complete power supply. Super junction transistors, fast Schottky diodes partially solved the efficiency problems by showing the promising results (Rossetto 1994). Introduction of fast switching GaN HEMT brought a revolution in field of PFC converters. In next section we will discuss how GaN HEMT makes it possible to operate Totem Pole PFC in CCM mode.

#### 3.6.1 Totem Pole PFC based on GaN HEMTs:

Totem pole PFC circuit is shown in Figure 42. Very low gate charge of GaN HEMT makes it possible to operate converter at very high switching frequencies. Very low reverse recovery and switching losses makes it possible to operate totem pole PFC in CCM after employing GaN HEMTs. CCM operated GaN HEMTs based Totem pole PFC

converter when operated in ZVS mode will increase the switching frequency range of converter (Xue, Shen et al. 2015).

Totem Pole PFC has two commutation legs. One of them is slow commutation leg that operates at line frequency while the other one is high frequency commutation line which operates at switching frequency. Figure 42 shows the implementation of circuit by two MOSFETs and two diodes. MOSFETs will be replaced by GaN HEMTs that will constitute high commutation leg and In order to further boost efficiency of circuit, two diodes in slow commutation leg will be replaced with MOSFETs having very low drain to source to resistance (GaN 2013).

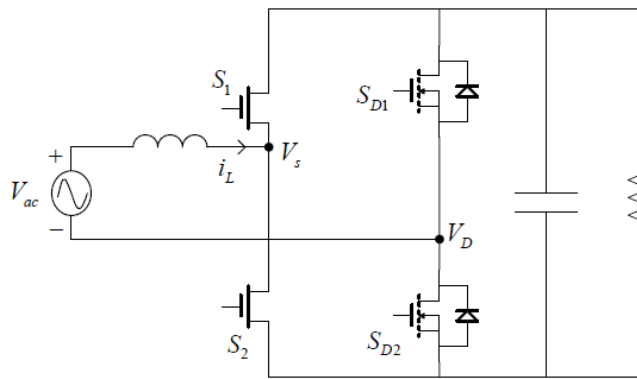


Figure 43: Totem Pole PFC - With MOSFETs for Line Rectification (Zhou, Wu )

This circuit is similar in operation as that in Figure 42, the only difference is addition of MOSFETs  $S_{D1}$  and  $S_{D2}$ .

In spite of all merits, this circuit inherits a problem of current spike at every zero crossing of supply voltage. Every time when supply voltage will change its polarity from positive to negative, duty ration of switch  $S_2$  will vary from 100% to 0% and that of switch  $S_1$  will vary from 0% to 100%. Due to slow response of body diodes, voltage  $V_D$  cannot jump to the level of output DC voltage level  $V_{DC}$  instantly, which will give rise to current spike at every zero crossing. Soft start for switches at every zero crossing is incorporated in circuit which resolves the problem of current spike but in turn complicates the control design. However converter operating in CCM has fairly large inductance which can eliminate the current spike at zero crossings but still soft start is employed for first few cycles to completely avoid the current spike (Zhou, Wu ).

Overall control circuit can be shown as:



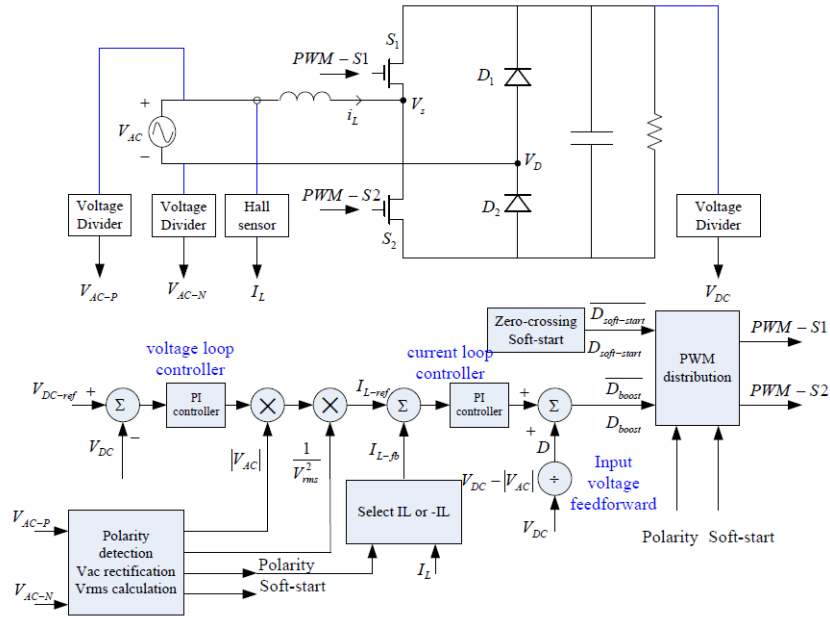


Figure 44: Control Circuit of Totem Pole PFC in CCM (Zhou, Wu )

This control circuitry is for converters with line frequency diodes in slow commutation legs. Voltage and current loops of control system are similar to those in conventional Boost converter PFC. Detailed information about all feedback signals is being given in previous sections. In order to avoid current spikes soft start duty ratio is used for very short period after every zero crossing. With addition of MOSFETs in slow commutation leg will require two more gate driving signals. Timing diagram for MOSFETs can be shown as:

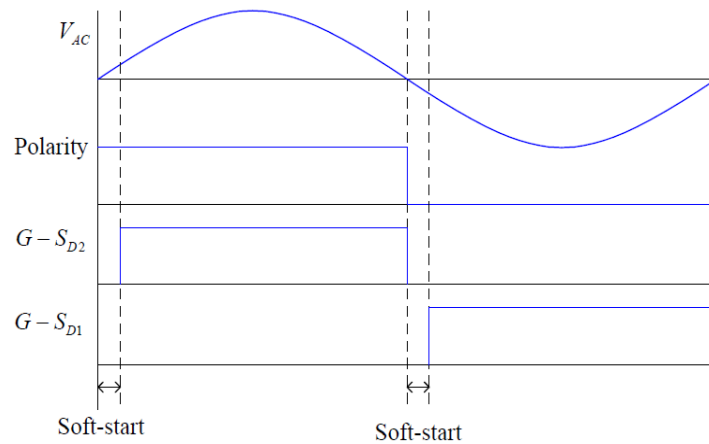


Figure 45: Gate signals for line rectification MOSFETs (Zhou, Wu )

During soft start period, both MOSFETs are in OFF state and they behave like simple diodes (Zhou, Wu ).

### 3.7 Simulation of Conventional Bridged Boost Converter PFC:

We have been discussing about the impact of wide band gap devices on various Power Electronics applications. Indeed PFC circuits are one of the best applications of WBG. To support our discussion and to investigate the effect of WBG switch on PFC circuit, a simulation is being carried out.

In our next section we will discuss the experimental results of tests being performed on EZ-GaN Evaluation Board, All-in-One Power Supply by Transphorm USA. In order to have a comparison between simulation and experimental results, this PFC circuit was designed to operate at same switching frequency as that of Power Supply Unit.

Simulation was done on LTspice IV. This software does not need any license and is available free of cost. It takes the non-idealities of components in to consideration and results are comparable to practical results.

Conventional bridged PFC circuit was chosen for this simulation. This circuit was chosen because of following reasons:

- Widely accepted PFC circuit and being used in many practical applications.
- Simple and convenient control circuit.
- Integrated control circuit available.
- Convenient operation in CCM.

Main purpose of this simulation was to compare the performance of PFC circuit with different Boost switches. To compare the performance of PFC circuit Transphorm 600 V GaN HEMT TPH3002, Cree 1200 V SiC MOSFET and Infenion 650 V SPA11N60C3 Si MOSFET were being chosen. Data sheets of these switches can be found in Appendix B, C & D respectively.

#### 3.7.1 Comparison of Boost Switches:

Following table will give us the brief comparison of different Boost switches that were being chosen for the simulation.

*Table 2: Boost switches Comparison*

|                        | <b>TPH3002</b> | <b>C2M0280120D</b> | <b>SPA11N60C3</b> |
|------------------------|----------------|--------------------|-------------------|
| $V_{DS}$ (V)           | 600            | 1200*              | 650               |
| $I_D$ (A)              | 9              | 10                 | 11                |
| $R_{DS}$ (m $\Omega$ ) | 290            | 280                | 380               |
| $Q_g$ (nC)             | 6.2            | 20.4               | 45                |
| $Q_{rr}$ (nC)          | 29             | 70                 | 6000              |
| $t_{rr}$ (ns)          | 30             | 24                 | 400               |

\*600 V SiC MOSFET was not available, this model was chosen because  $R_{DS}$  and  $I_D$  are almost similar to GaN HEMT and Si MOSFET.

### 3.7.2 Circuit Parameters:

PFC circuit has the following Parameters.

*Table 3: PFC Circuit Parameters*

|                          |                         |
|--------------------------|-------------------------|
| Input Voltage            | 230 Vac 50Hz            |
| Output Voltage           | 400 VDC                 |
| Inductor Current Ripple  | 30% @ Full load current |
| Switching Frequency      | 200 kHz                 |
| Steady State Power       | 250 Watts               |
| Output DC Ripple Voltage | 20 VDC                  |

### 3.7.3 Circuit Design:

In this section we will briefly describe the design procedure of simulation circuit.

Design procedure consists of two sections.

- Design of Power stage.
- Design of Control circuit.

### 3.7.4 Design of Power stage:

Reference design for design of Boost Converter is being taken from (Stückler 2014). Power Stage of PFC circuit includes the design of Boost Inductor, Rectifier Diodes, MOSFET, Shotkey Diode and Output Capacitor.

#### 3.7.4.1 Boost Inductor:

Boost Inductor specifies the mode of operation of converter. For CCM inductor value in terms of maximum permissible inductor ripple current is given by (Stückler 2014):

$$L = \frac{1}{\%Ripple} * \frac{Vac^2}{P_o} * \left(1 - \frac{\sqrt{2}Vac}{V_o}\right) \cdot T = 658.87 \mu H \quad (3-11)$$

Maximum current through inductor can be given as (Stückler 2014):

$$I_{LMax} = \frac{\sqrt{2}P_o}{Vac} \cdot \left(1 + \frac{\%Ripple}{2}\right) = 1.76A \quad (3-12)$$

The saturation level for Boost inductor should be greater than 1.76A. Hence, inductor with inductance of 680  $\mu H$  and saturation current of 2A is chosen for simulation.

#### 3.7.4.2 Rectifier Bridge:

Average current flowing through rectifier each supply cycle can be calculated as (Stückler 2014):

$$I_{average} = \frac{2}{\pi} \cdot \frac{\sqrt{2}P_o}{V_{ac}} = 0.978A \quad (3-13)$$

Forward drop can be minimized by choosing the diode with higher current rating (Stückler 2014). Rectifier diode CHD8-06 from Central Semiconductor with rated current of 8A and rated blocking voltage of 600V was chosen for the simulation model.

#### 3.7.4.3 Boost Diode:

Boost diode has a significant role in performance of converter. As Boost diodes are switched at high currents, so reverse recovery can increase the overall losses and current spikes may also contaminate the line with electrical noise. Reverse recovery characteristics of a diode can certainly put a limit over the maximum switching frequency and power density of the converter. Hence, decision of choosing Boost diode is very critical in design of converter.

As explained in previous sections, SiC Shotkey diodes are far superior in their performance over Silicon Ultra-fast diodes. That is the reason for using SiC Shotkey diode from CREE with rated current of 5A and DC blocking voltage of 600 V in simulation.

#### 3.7.4.4 Output Capacitor:

To have smooth filtered DC voltage at output a Bulk capacitor is used. Value of capacitor depends upon the frequency of ripple and allowed ripple voltage. As in our requirement ripple frequency is 100Hz (twice as mains frequency) and allowed ripple voltage is 20V.

$$C > \frac{P_o}{2\pi f_{line} V_{ripple} V_o} = 99.47 \mu F \quad (3-14)$$

Hence to be at safer side, capacitor with capacitance of 180μF was chosen for simulation. RMS value of capacitor current can be estimated by following equation (Stückler 2014):

$$I_{co} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot P_o^2}{(3 \cdot \pi \cdot V_{ac} \cdot V_o)} - \frac{P_o^2}{V_o^2}} = 0.652 A \quad (3-15)$$



$$f_{sw} = \frac{1.5}{R_{set}C_{set}} \quad (3-16)$$

Capacitor of capacitance 0.50 nF was chosen. As required switching frequency is 200 kHz, so according to equation above, value of resistance comes out to be 15 kΩ.

#### 3.7.5.2 Maximum Line Current Limit:

This control IC has feature of limiting the line current to specified value. Value of line current is restricted by sensing resistor  $R_s$  in Figure 46. In our simulation value  $R_s$  is 0.2 Ω to limit the maximum line current to 5 A. Detailed calculation of  $R_s$  value can be found in Appendix A.

#### 3.7.5.3 Output Voltage Regulation:

In LT1509 output voltage is continuously being compared with reference voltage of 7.5 V. If voltage exceeds the reference voltage, it shuts down the gate driving circuit. Usually a resistance divider circuit is employed at the output of the circuit. As our desired output voltage level is 400 V, so we had to design divider circuit in such a way that it gives 7.5V for 400 VDC. Calculations for divider circuit can be found in Appendix A.

#### 3.7.5.4 Voltage Error Amplifier:

Voltage error amplifier has a Dc gain of 100 dB and can operate with unity gain up to 3MHz.

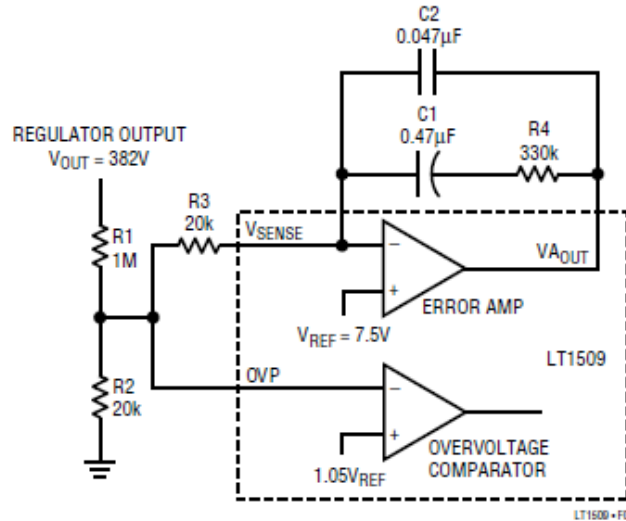


Figure 47: Voltage error Amplifier (Linear Technology 1994)

Error amplifier is basically comparing the voltage level at  $V_{SENSE}$  pin with reference voltage in order to regulate the output voltage. In our simulation model we sue the

same values of resistors and capacitors for the stable operation of amplifier. Gain for this amplifier can be given as:

$$\frac{VA_{out}}{V_{out}} = - \frac{1 + j\frac{f}{1}}{j * f * 6.6 * \left(1 + j\frac{f}{11}\right)} \quad (3-17)$$

Gain and Phase margin of amplifier is given by following figure:

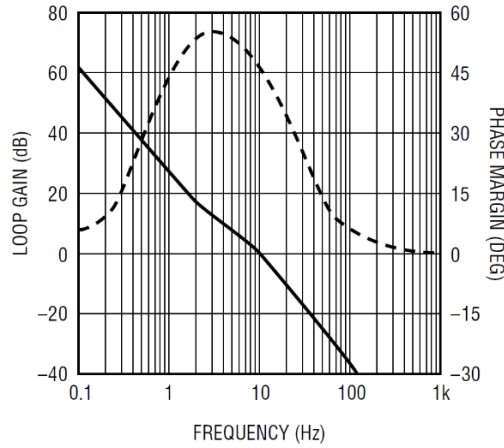


Figure 48: Phase and Gain Margin of Voltage Amplifier (Linear Technology 1994)

At very low frequencies, amplifier has -40 dB/decade slope. Unity gain at frequencies lower than 120 Hz results in low distortion and high power factor (Linear Technology 1994).

Overvoltage comparator is comparing the output voltage through voltage divider with 1.05 times of  $V_{REF}$ , hence when scaled output voltage will increase more than the 1.05 times of reference voltage it will turn OFF the gate signal.

#### 3.7.5.5 Current Amplifier:

Current Amplifier of PFC controller has DC gain of 110 dB and has unity gain frequency of 3MHz.





$$V_{est}(f_D)[dB\mu V] = 20.\log\left(\frac{V_{hrms}}{m} \cdot \frac{1}{10^{-6}}\right) = 166 \text{ dB}\mu V \quad (3-20)$$

However, according to the standards, conducted emissions level at 200 kHz should be lesser than 64 dB $\mu$ V (Mühlethaler, Uemura et al. 2012). So we need to have filter with attenuation of more than 100 dB $\mu$ V.

Design of filter requires to take 26 many physical factors in to account. As our main goal is to study the effect of different boost switches, so we decided not to go in to the details of filter design. According to our reference design in (Mühlethaler, Uemura et al. 2012), one way to estimate the noise is to monitor the high frequency components of voltage across the switch.

Following image shows the values of the filter components chosen for our simulation model.

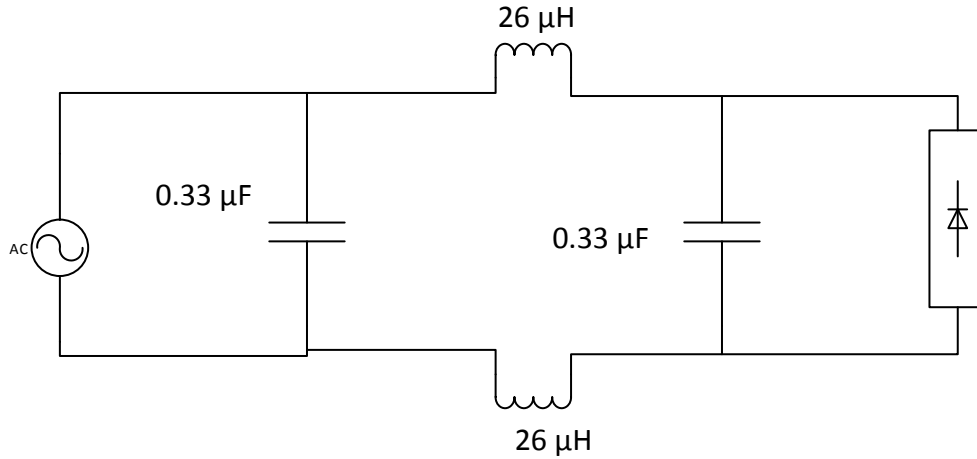


Figure 50: DM Noise Filter

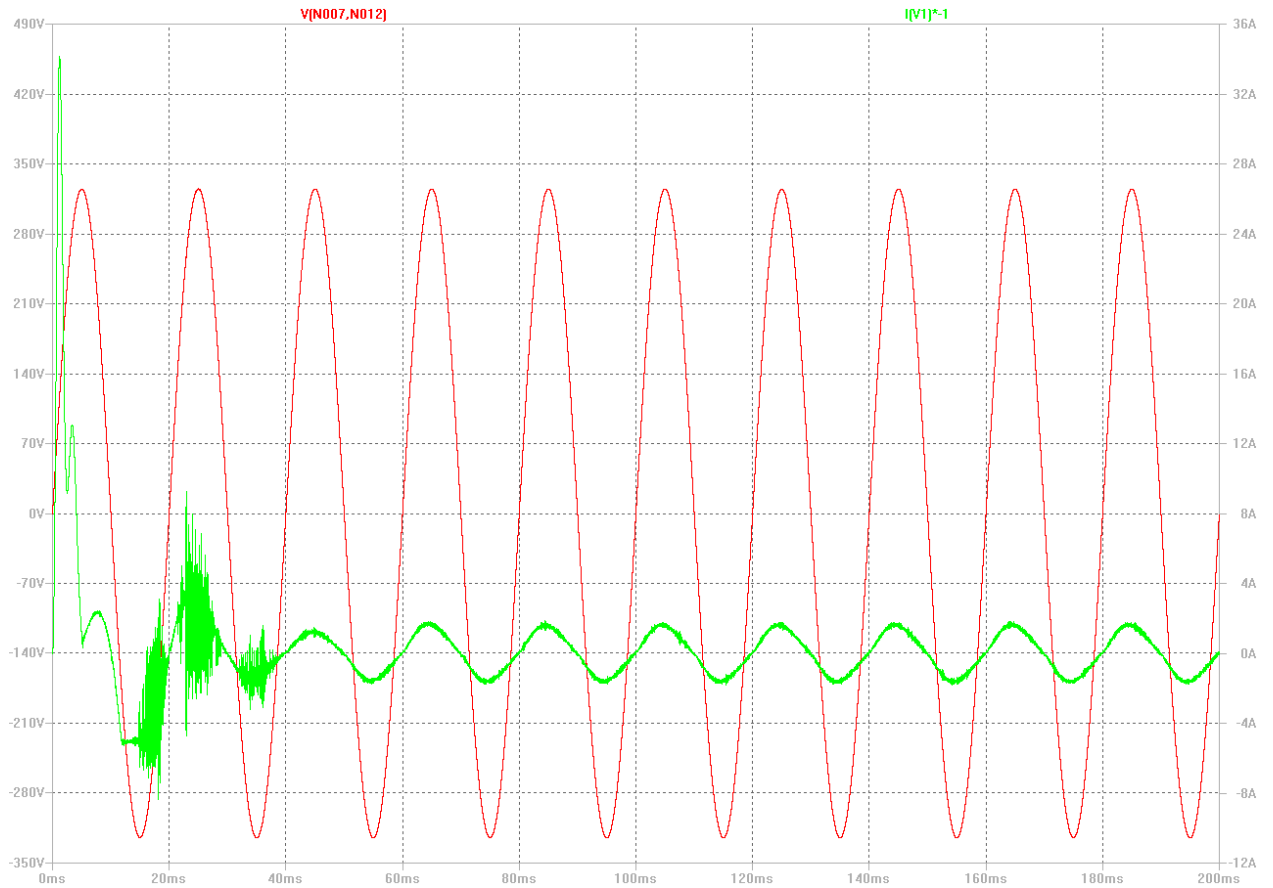
High frequency component of voltage across the switch was observed to evaluate the performance of filter. Results showed the satisfactory performance of chosen filter components. FFT analysis of voltage across the switch is shown in Figure 52.

### 3.9 Results:

As described above, the motive of this simulation was to compare the performance of Si MOSFET, SiC MOSFET and GaN HEMTs. In this section we will discuss the main results of simulation.

### 3.9.1 Input Current Shaping:

Power factor correction capability of circuit does not depend the type of switch being used. Shaping of input current depends upon the control circuit that is being employed in the circuit. In all three circuits, average current mode was being used. So results for all three circuits will be identical.



*Figure 51: Input Current and Voltage Waveform*

High Current spikes in first couple of cycles is due to charging of output bulk capacitor. High current spike at the beginning can be avoided by using soft starting techniques.

### 3.9.2 Fourier Transform of Voltage across the switch:

Noise generated by the circuit can be estimated by the level of high frequency components of voltage across the switch. To visualize the high frequency voltage components FFT analysis of switch voltage was obtained. Low level of high frequency components ( 40 dB) ensures the satisfactory performance of input filter.

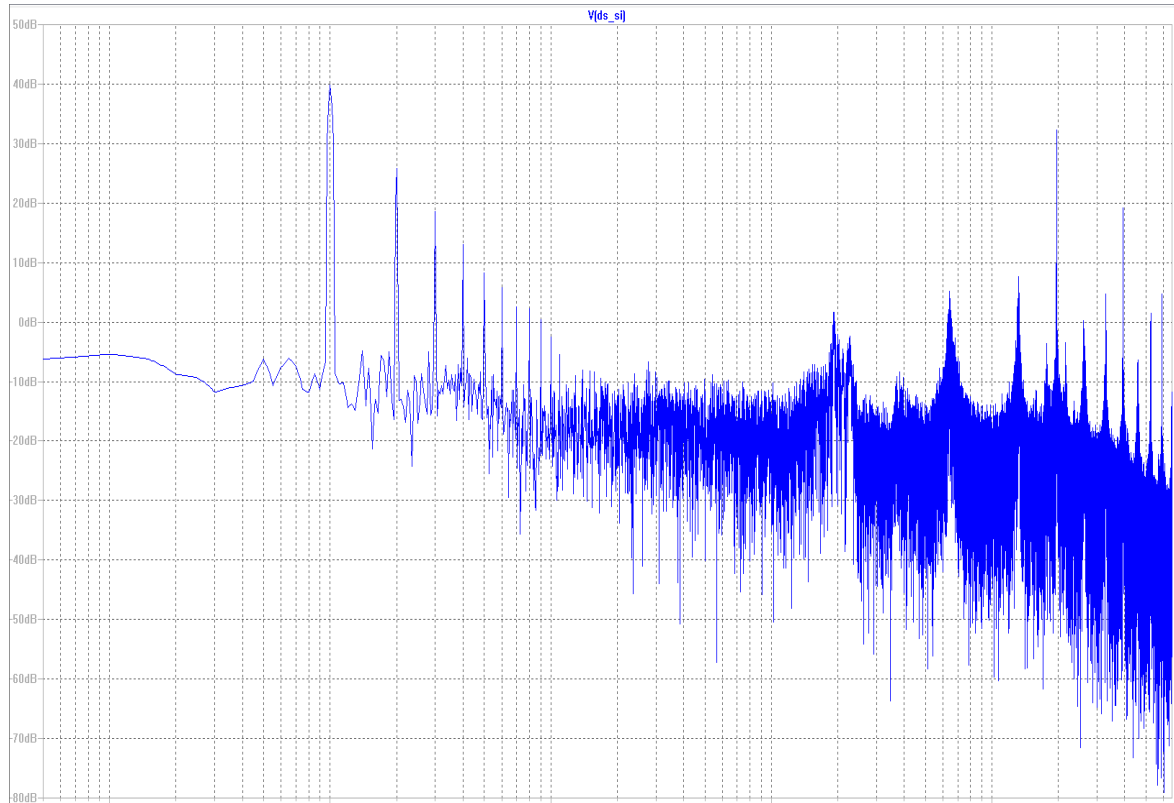


Figure 52: FFT of Voltage across switch (Si Switch)

### 3.9.3 Boost Diode Performance:

SiC Diode exhibit excellent characteristics with almost zero reverse recovery. Current waveform through diode was observed to be same in all three circuits. Power Drop across the diode can be estimated by Figure 53.

LTspice has the function which can take product of two waveforms. To estimate the power drop across the diode we can simply take product of current passing through diode and voltage across it.

Order for the waveforms will be maintained as in previous section i.e. first waveform will be from circuit with GaN switch, second from circuit with SiC switch and third from circuit with Si switch.

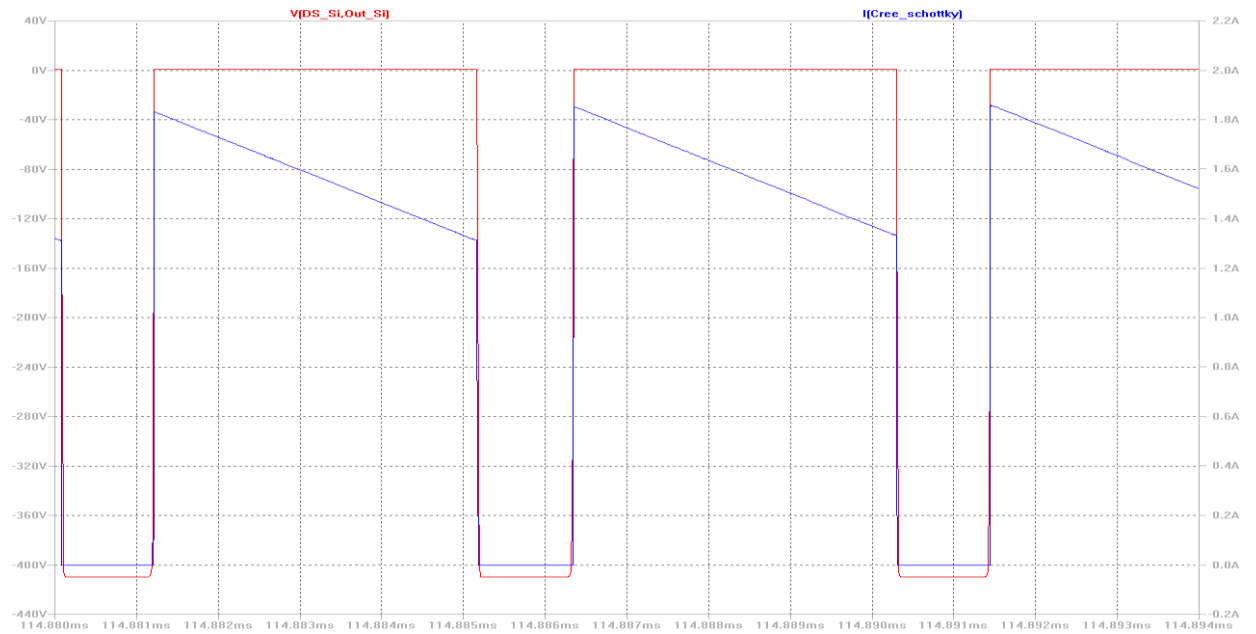


Figure 53: Boost Diode Current and Voltage (Si Switch)

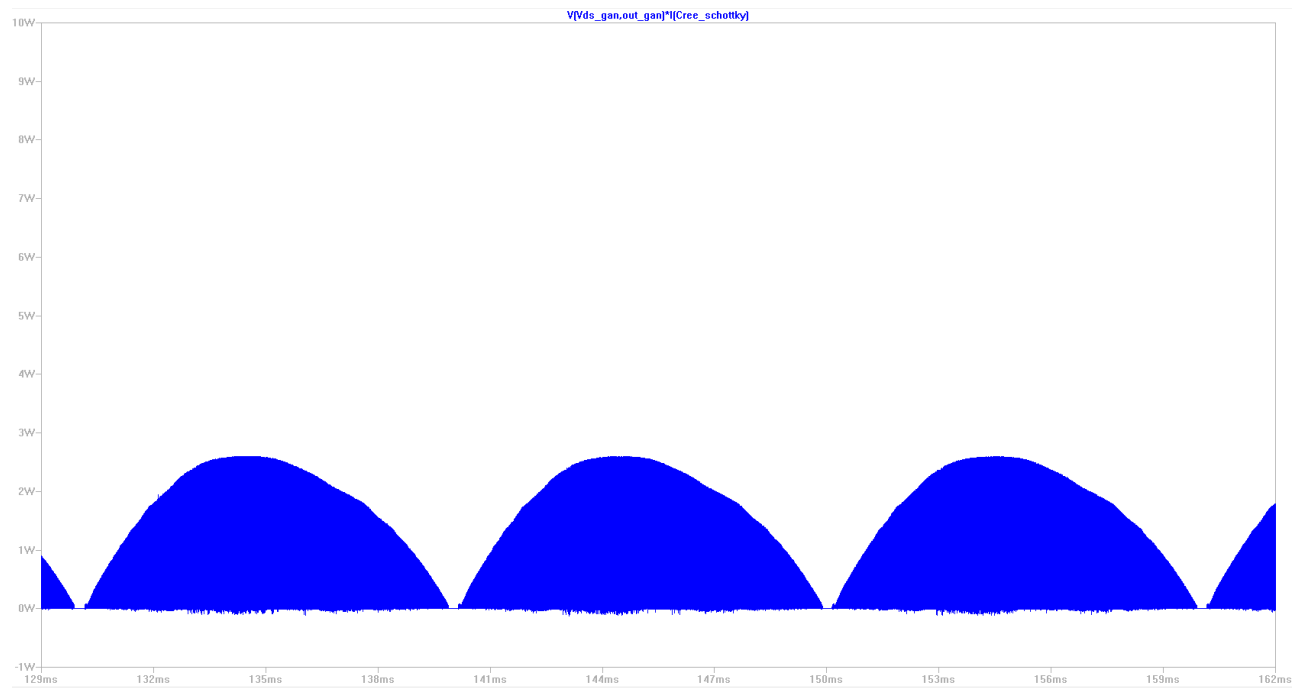


Figure 54: Boost Diode Power Drop (W) (GaN Switch)

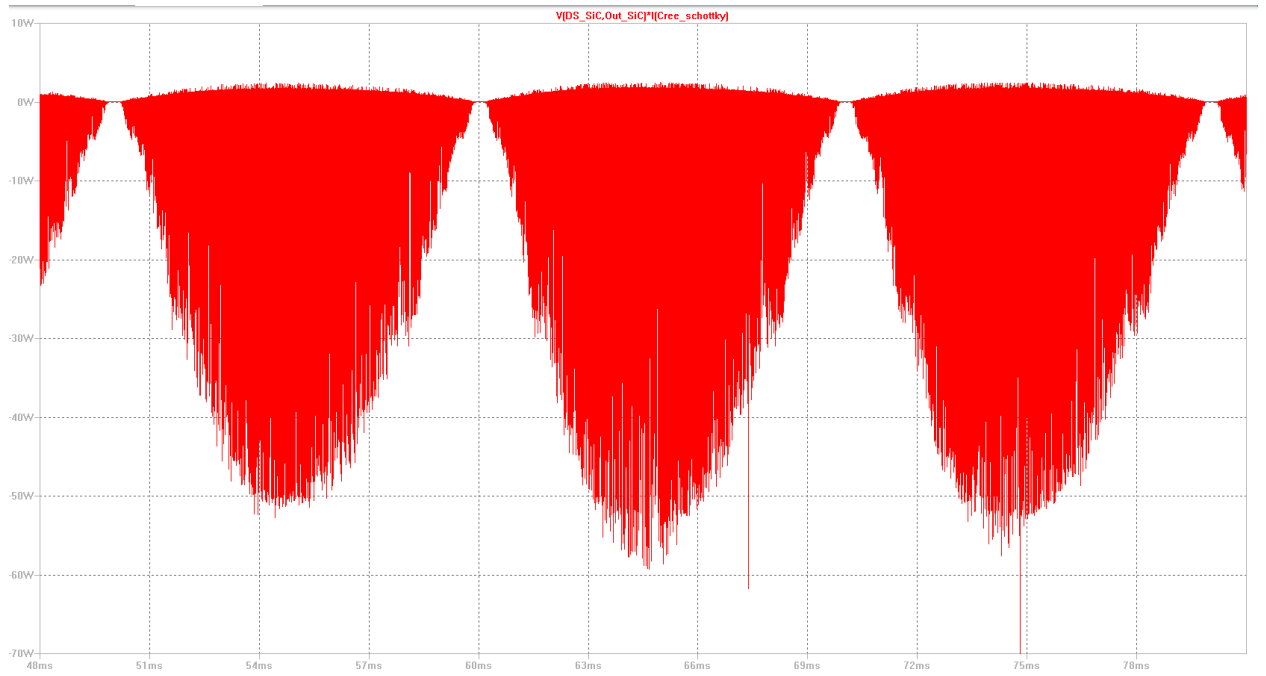


Figure 55: Boost Diode Power Drop (W) (SiC Switch)

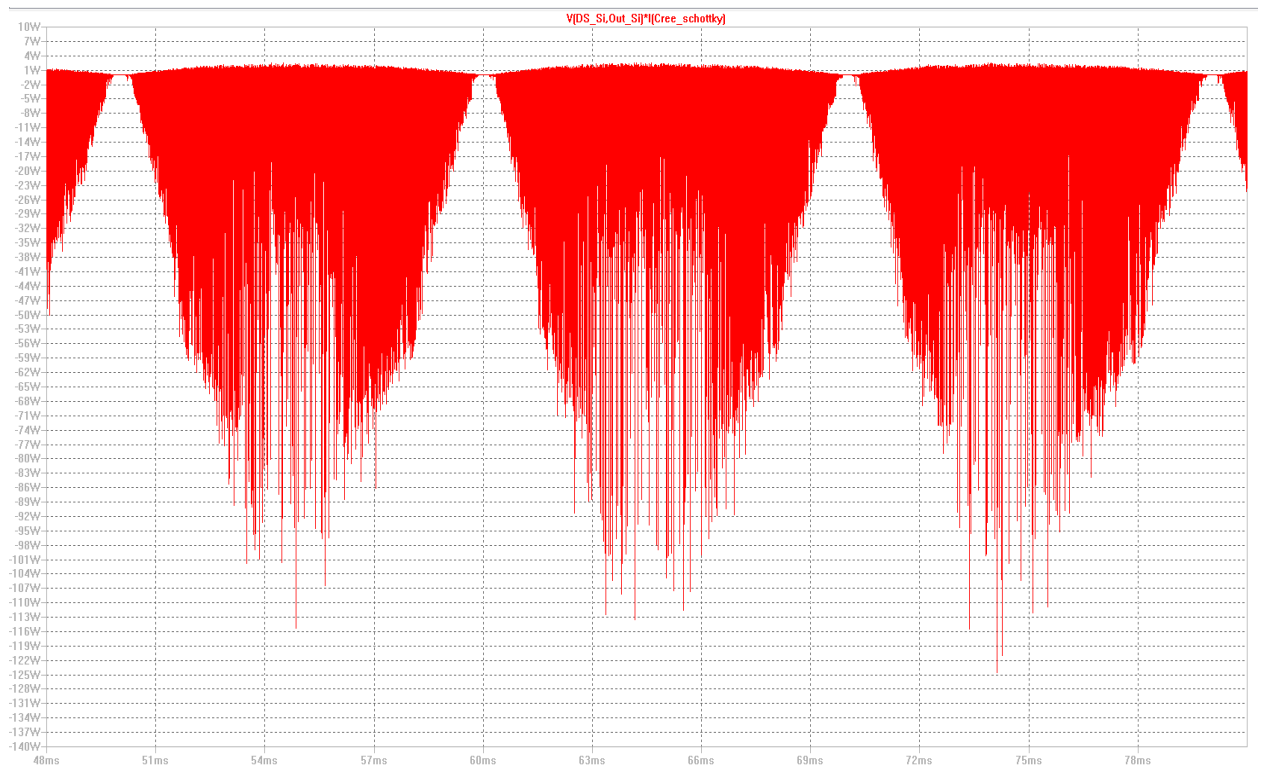


Figure 56: Boost Diode Power Drop (W) (Si Switch)

Positive peak in power loss diagrams accounts for conduction losses or forward drop. Conduction losses for all three cases would be same, as it depends upon the characteristics of diode. However, negative peaks defines the performance of power switch. During switching OFF of boost diode, voltage across it (anode to cathode) will become negative i.e. equal to reverse blocking voltage which in our case is 400 VDC. Voltage across the diode cannot change instantly. So the time that will be taken by diode to develop 400 VDC across it depends upon the switching ON speed of power switch. Negative power drop appears because of presence of both current and negative voltage during the switching transition of diode.

Huge difference of power loss across diode between three circuits is because of difference in their switching speeds. Circuit with GaN switch has minimum losses across Boost diode as it is the fastest one among these three switches. In next section we will calculate the turn ON and OFF times of switches to compare their switching losses.

#### 3.9.4 Switching Characteristics:

Switching characteristics include turning ON and OFF of switch. In order to incorporate the switching losses as well in this section, we will add a third waveform i.e. product of Drain to source voltage and Drain current that will represent switching losses.

##### 3.9.4.1 Switching ON Waveforms:

In all three waveforms, red curve is product of drain to source voltage and drain current i.e. it represents the switching ON losses across the switch. Green and blue curves are drain to source voltage and drain current respectively. These waveforms give the visualization of switching ON of respective power switch.

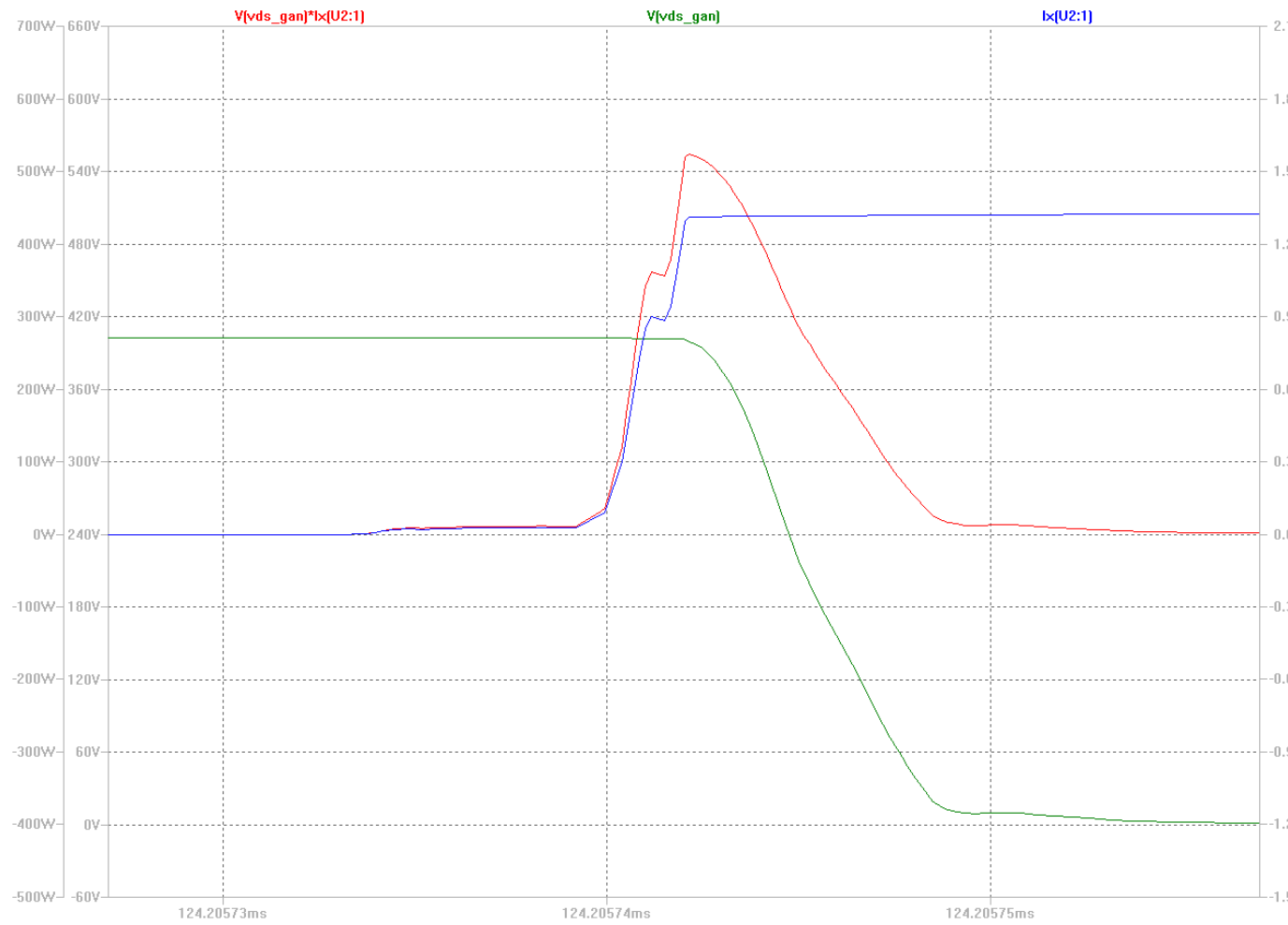


Figure 57: Turn ON waveforms (GaN Switch)

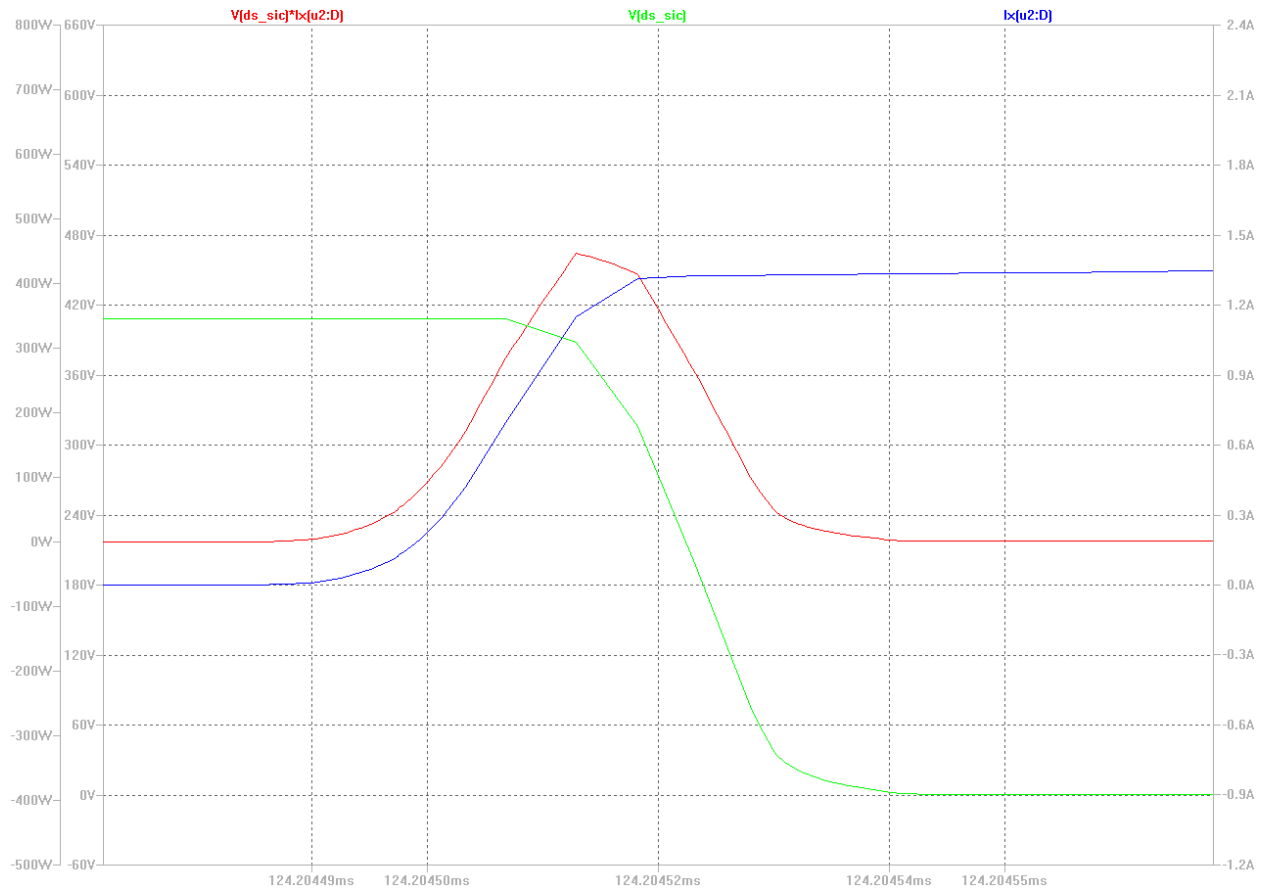


Figure 58: Turn ON waveforms (SiC Switch)

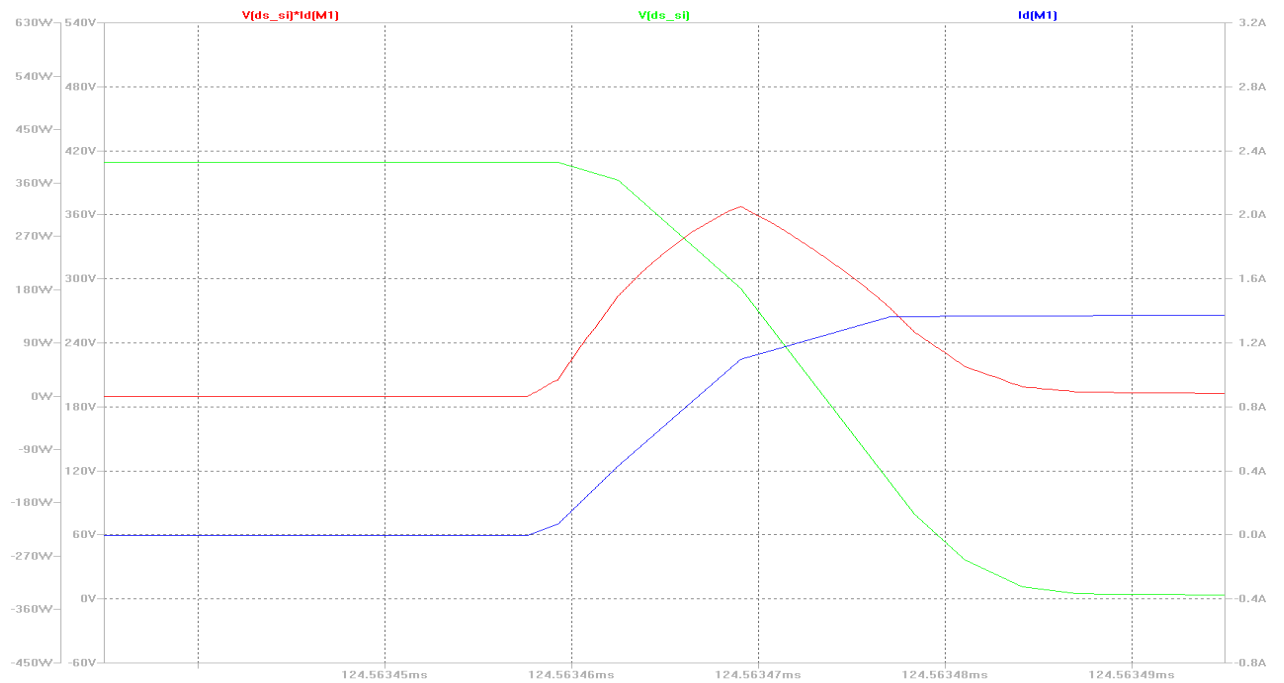


Figure 59: Turn ON waveforms (Si Switch)



### 3.9.4.2 Switching OFF Waveforms:

In all three waveforms, red curve is product of drain to source voltage and drain current i.e. it represents the switching OFF losses across the switch. Green and blue curves are drain to source voltage and drain current respectively. These waveforms give the visualization of switching OFF of respective power switch.

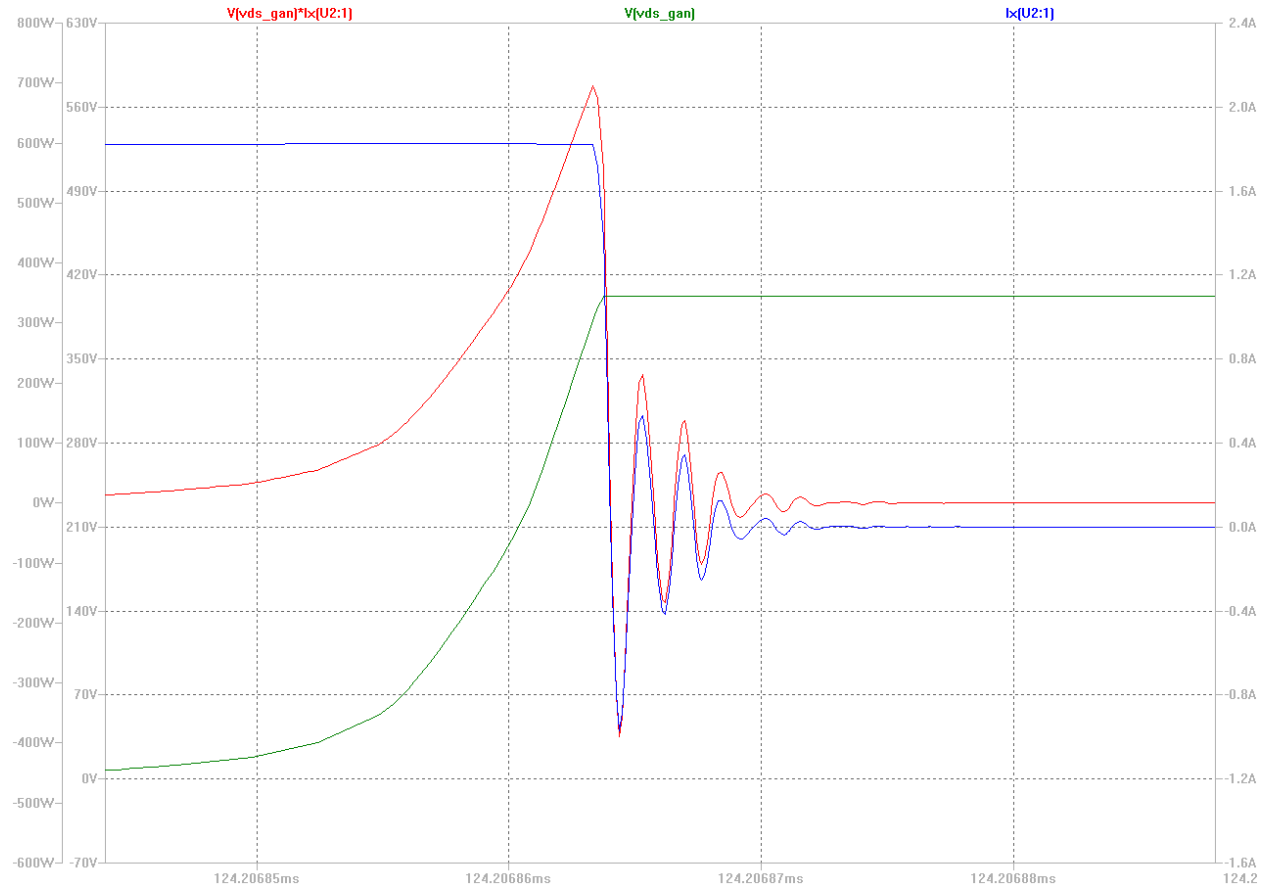


Figure 60: Turn OFF waveforms (GaN Switch)

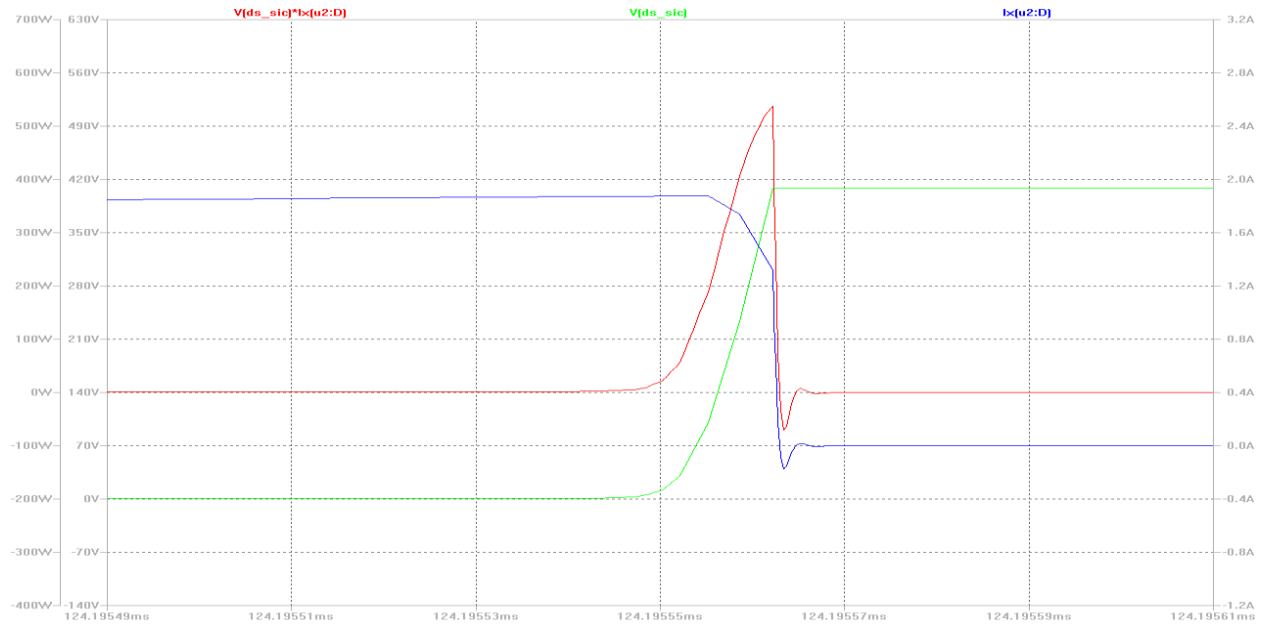


Figure 61: Turn OFF waveforms (SiC Switch)

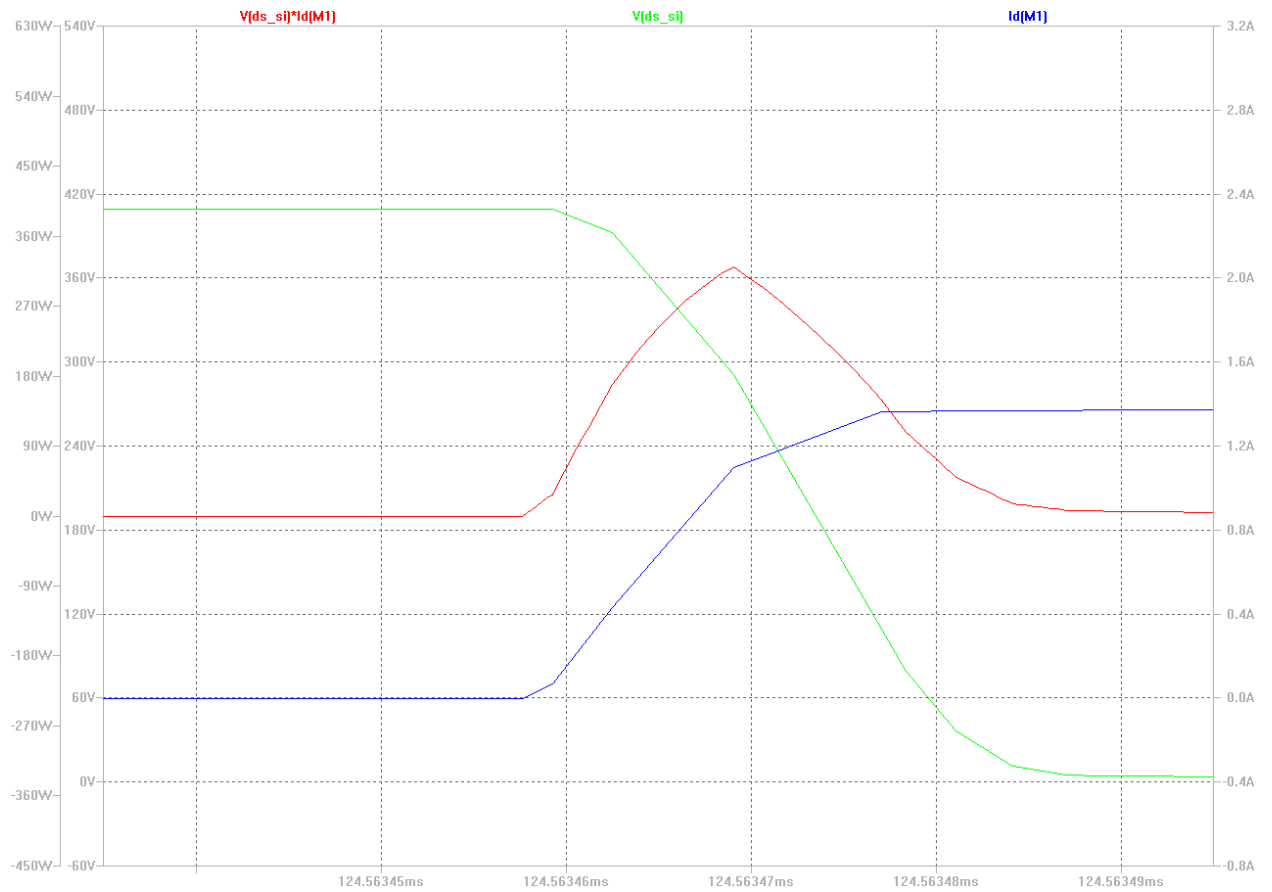


Figure 62: Turn OFF waveforms (Si Switch)

Ringing effect was observed in GaN HEMT current waveform during its switching OFF transition. As circuit was simulated Ultra-fast response of GaN HEMTs with parasitic inductances in the circuit is the reason behind this ringing effect.

Turn ON and OFF times of switches under identical gate driving and output load conditions:

*Table 4: Switching Times of switches*

| Switch Material | ON Time (ns) |           | OFF Time (ns) |           |
|-----------------|--------------|-----------|---------------|-----------|
|                 | Data Sheet   | Simulated | Data Sheet    | Simulated |
| GaN             | 4            | 30.4      | 4.5           | 15.9      |
| SiC             | 7.6          | 35.7      | 9.9           | 37.6      |
| Si              | 5            | 40.8      | 5             | 34.9      |

Slow rise and fall time of controller slowed the response of switches as well. The controller that we used for our simulation was with rise and fall time of 25 ns.

As described above, due to very low gate capacitance GaN HEMT is undoubtedly the fastest switch.

### 3.9.5 Switching Loss Comparison:

Switching losses are categorized as the major contributor in overall losses of a converter. Here we will compare the average of switching losses for each circuit. As our circuit is working with automated variable duty cycle, hence it is not possible to calculate the switching losses theoretically. One way to estimate the average switching losses is to take average of product of drain to source voltage and drain current. LTspice has this function. Hence, average of loss waveform was computed for the time duration of 170ms (30ms ~ 200ms).

*Table 5: Switching Loss Comparison*

| Switch | Avg. Switching losses (W) | % Loss Reduction |
|--------|---------------------------|------------------|
| Si     | 1.7588                    |                  |
| SiC    | 1.6294                    | 7.35%            |
| GaN    | 1.0848                    | 38%              |

% loss reduction was calculated on the basis of losses in converter with Si Switch.

## Chapter 4. LLC Resonant Converter:

### 4.1 Introduction:

In modern day power supplies it is desirable to use higher switching frequencies to reduce the size of magnetic components. However, increasing switching losses are obstacle in the way of employing high switching frequencies. With increasing demands of highly efficient power electronic circuits, many techniques have been introduced to reduce the switching losses. In previous chapters, we have discussed that how switching losses can be reduced by employing Wide band Gap power devices. However, WBG technology still needs to get matured with time.

In power MOSFET, switching losses occur due to charge stored in output capacitance ( $C_{oss}$ ). When the MOSFET is switched OFF, it blocks heavy voltage which results in charging up the output capacitance of FET. When MOSFET is turned ON this FET delays the switching ON time due to discharge of  $C_{oss}$  which results in significant power loss that increases at higher switching frequencies.

Resonant circuits provide us with the solution to avoid these losses. Resonant converters are in the field of highly efficient power electronics for more than 30 years. Basically in resonant converters switches are commuted softly to achieve zero voltage switching (ZVS) in order to reduce the losses across them (Semiconductor 2007). Resonance is achieved by resonant tank including magnetic components. ZVS is achieved by discharging the  $C_{oss}$  across the resonant tank and MOSFET is turned ON after the voltage across it has dropped to zero.

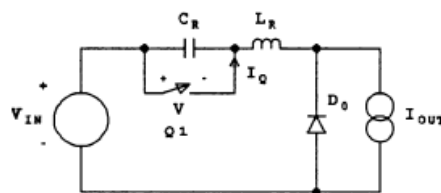


Figure 63: Basic Resonant Switch (Semiconductor 2007)

Figure 63 shows the implementation of simple resonant switch. In this circuit,  $C_R$  and  $L_R$  constitutes the resonant tank. This circuit is also termed as series LC circuit, as both  $C_R$  and  $L_R$  are in series with each other. One way to look at this circuit is that the resonant tank is in series with load. So by varying the switching frequency we can vary the impedance of resonant tank to regulate the output voltage (Semiconductor 2007). When the switch is turned ON ideally there should not be any drop across it, hence  $C_R$  gets short circuited and voltage across the capacitor will be zero. Current

will flow through FET,  $L_R$  and then to load, as diode  $D_o$  will not be conducting. When the switch is turned OFF, current through inductor will not drop to zero instantly. So current will flow through  $C_R$  to  $L_R$  and load. At this point resonance will be achieved by variable driving frequency operation and  $C_{OSS}$  will discharge across the resonant tank. Detailed analysis of ZVS operation can be found in (Andreycak 1990)

One drawback of this circuit is that at light loads, load impedance will be very large as compared to the impedance of resonant tank. In that case whole input voltage will appear across the load and it will become very difficult to regulate the output voltage. To overcome this problem, another shunt-inductance is being added in parallel to the load. This circuit is known as series LLC circuit (Figure 64). Most of the times in LLC circuit, the inductance of shunt inductor is incorporated with the inductance of transformer.

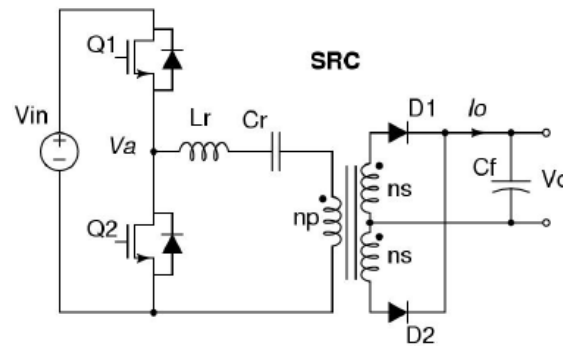


Figure 64: Series LLC circuit (Andreycak 1990)

The main difference between LC series resonant converter and LLC resonance converter is the value of series inductance. Usually in LLC converter, inductance value is realized by the magnetization inductance of transformer. Magnetization inductance in LLC converters is generally 3 to 8 times of  $L_R$  which is implemented by introducing more air gap in the transformer design (Semiconductor 2007).

These two circuits that we discussed above are examples of series resonant converters. However there are many topologies of resonant converters including ZVS Forward Converter, ZVS Full Bridge, Multi-resonant ZVS Conversion and Current Mode Controlled ZVS Operation that have been discussed and reviewed in many scholarly articles. We will only restrict ourselves to the operation and role of wide band gap power devices in Half Bridge series resonant converter.

## 4.2 LLC Half Bridge Resonant Converter:

Half Bridge Resonant converter plays a vital role in power supply design. Increasing demand of LLC half bridge converter is due to its highly efficient switching, very low noise and ability to achieve high power density. Figure 30 represents the basic block diagram of DC power supply. After PFC boost converter DC/DC converter is employed to step down the DC voltage to utility level. For this purpose many designers use half bridge resonant converter with rectifier at the output of resonant converter. Same topology is being used in Transphorm EZ-GaN All-in-One Power Supply.

LLC half bridge resonant converter consists of three portions i.e. square wave generator, resonant tank and synchronous Rectifier. Square wave is being generated with the help of Power FETs which is being fed to resonant tank consisting of  $L_R$  (Resonance Inductance),  $L_M$  (Magnetization Inductance) and  $C_R$  (Resonance Capacitor) as shown in Figure 64.

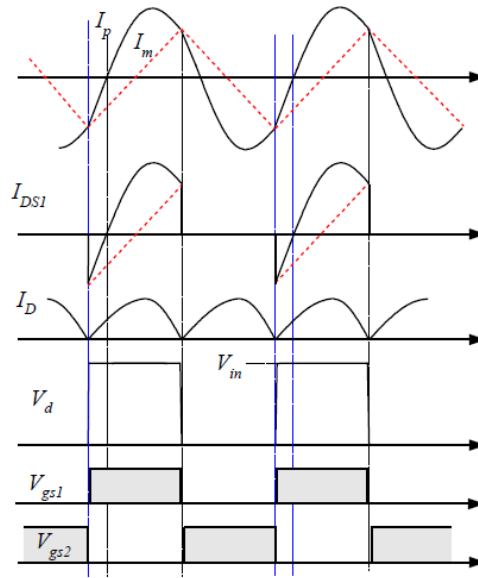


Figure 65: Waveforms for LLC Resonance Converter (Semiconductor 2007)

Where  $V_{gs1}$  : Gate Voltage for upper FET ,  $V_{gs2}$  : Gate Voltage for Lower FET,  $V_d$  : Voltage Across Lower FET,  $I_D$  : Output Load current ,  $I_{DS1}$  : Current Through Upper FET ,  $I_P$  : Primary Side current,  $I_m$  : Magnetization Current of Transformer.

Both FETs are driven complementarily with equal duty cycle ratios i.e. 50%, however gate control is based on variable driving frequency to regulate the output voltage. In spite of applying square wave voltage to resonant converter only sinusoidal current flows through it. When upper FET is switched ON, current  $I_P$  and  $I_m$  will start increasing and charging the resonance capacitor. As the current  $I_P$  lags the voltage applied across

the resonance tank, it makes it possible to switch ON the MOSFET when the voltage across it dropped to zero (Semiconductor 2007). Current free wheels through the antiparallel diode of lower MOSFET until the capacitor voltage reaches to its maximum value and it makes the current to flow in opposite direction. This AC current with square wave DC voltage is being applied to synchronous rectifier. Each diode in rectifier with center tap winding will conduct for one half cycle to generate DC output power.

DC gain of LLC resonant half bridge converter can be given as (Semiconductor 2007):

$$M = \frac{2nV_o}{V_{in}} \quad (4-1)$$

Where n is turn Ratio of transformer.

Dc gain at resonant frequency regardless of load variations should be unity (Semiconductor 2007).

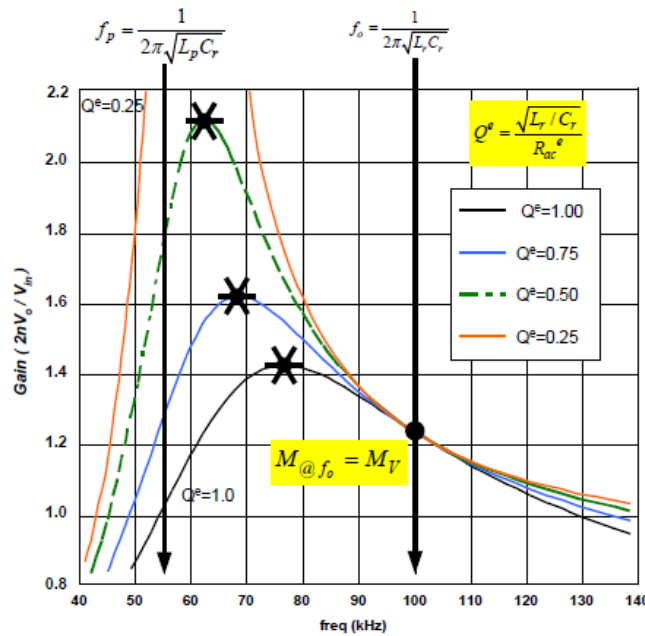


Figure 66: Frequency Response of LLC Half Bridge (Semiconductor 2007)

Figure 66 depicts the frequency response of LLC Half Bridge Circuit for different values of quality factor Q. Operation range of converter can be divided in to two regions:

- Inductive Region: Operation Region after peak gain frequency
- Capacitive Region: Operation Region before peak gain frequency.

For the ease of driver control circuit design and voltage regulation, it is desirable to operate the converter at switching frequencies in inductive region (Hsieh, Tsai et al. 2007). Another drawback of operating in capacitive region is that realization of ZVS will no longer be possible.

In frequency response of LLC converter,  $f_o$  represents the dominant resonant frequency which is inheritably a function of  $L_R$  and  $C_R$  and  $f_p$  is second resonant frequency that depends on  $L_M$  and  $C_R$  (Hsieh, Tsai et al. 2007).  $f_p$  is also termed as no load resonance frequency and  $f_o$  is regarded as full load resonance frequency. Usually input of LLC Series Resonant circuit is being fed by PFC circuit output voltage which is normally regulated at 400V. Hence, most of the LLC converters are designed to operate at resonance frequency with fixed gain equal to unity. At resonant frequency ZVS is achieved for devices at primary side and ZCS is achieved for devices at secondary side of transformer. (Bing Lu, Wenduo Liu et al. 2006). Converter operating at switching frequency less than dominant resonant frequency will have more circulating current that will increase the internal losses of converter but secondary side diodes will get softly commutated which will eliminate reverse recovery losses of secondary side diodes.. However for switching frequency greater than resonant frequency, circulating currents will reduced immensely but diodes will not get softly commuted. So high voltage applications including Plasma Display Panel TV utilizes LLC converter operating at frequency less than resonance frequency while low voltage LCD TV incorporates converter with switching frequency higher than resonance frequency (Semiconductor 2007).

#### 4.3 GaN HEMT Based LLC Converter:

In LLC converter, during dead-time output capacitance of switches gets discharged to achieve ZVS switching. So dead-time should be long enough to provide enough time to achieve ZVS, but larger dead-time will result in inefficient energy transfer from primary to secondary side. Apart from output capacitance of switches, transformer windings at primary side also introduces parasitic capacitance. So total capacitance that needs to get discharged during dead-time would be the sum of output and parasitic capacitances. GaN HEMTs with exceptionally low output capacitance serve as the best candidate for LLC circuits.

Another factor that effects the discharging of capacitances is magnetization current. Relationship of magnetization current and dead-time with overall capacitances can be given as (Zhang, Xu et al. 2013) :

$$2T_{Co}V_{in} + \frac{2nQ_{osssr}}{n} + V_{in}C_w = I_m t_d \quad (4-2)$$



Where  $V_{in}$  is input voltage,  $T_{Co}$  is time related to effective output capacitance,  $Q_{oss_{sr}}$  is output charge of secondary side switches,  $n$  is number of semiconductor devices on secondary side of transformer,  $n$  is turn ratio of transformer,  $C_w$  is capacitance of windings,  $I_m$  is magnetization current and  $t_d$  is dead time.

Choosing higher magnetization current will result in higher conduction losses across the switching devices. So it is always a tradeoff between magnetization current and dead time. As we can see in equation (4-2) that output charge of synchronous rectifier switches is being divided by turn ratio of transformer, which means that dominant factor in equation will be  $C_{o(tr)}$  and  $C_w$ . A comparative study of GaN HEMT and Si CoolMOS in LLC Converter was carried out by (Zhang, Xu et al. 2013). Both Si and GaN based circuits were implemented with same transformer and hence have the same  $C_w$ . 57 ns switching off time was observed for 600 V GaN HEMT, however under similar loading conditions Si CoolMOS took 95 ns to get switched off. Lesser switching off time of GaN HEMT allows to choose smaller dead-time for LLC circuit which will result in effective transfer of energy from primary to secondary side.

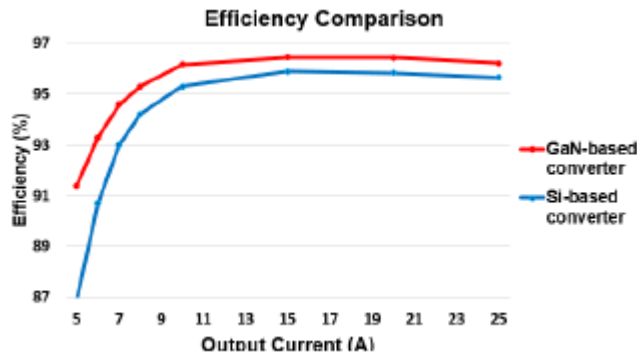


Figure 67: Efficiency Comparison of Si and GaN Based LLC Converter (Zhang, Xu et al. 2013)

By just replacing the Si CoolMOS with GaN HEMT 42% reduction in overall losses and 0.5% improvement in efficiency of converter was observed (Bing Lu, Wenduo Liu et al. 2006, Zhang, Xu et al. 2013).

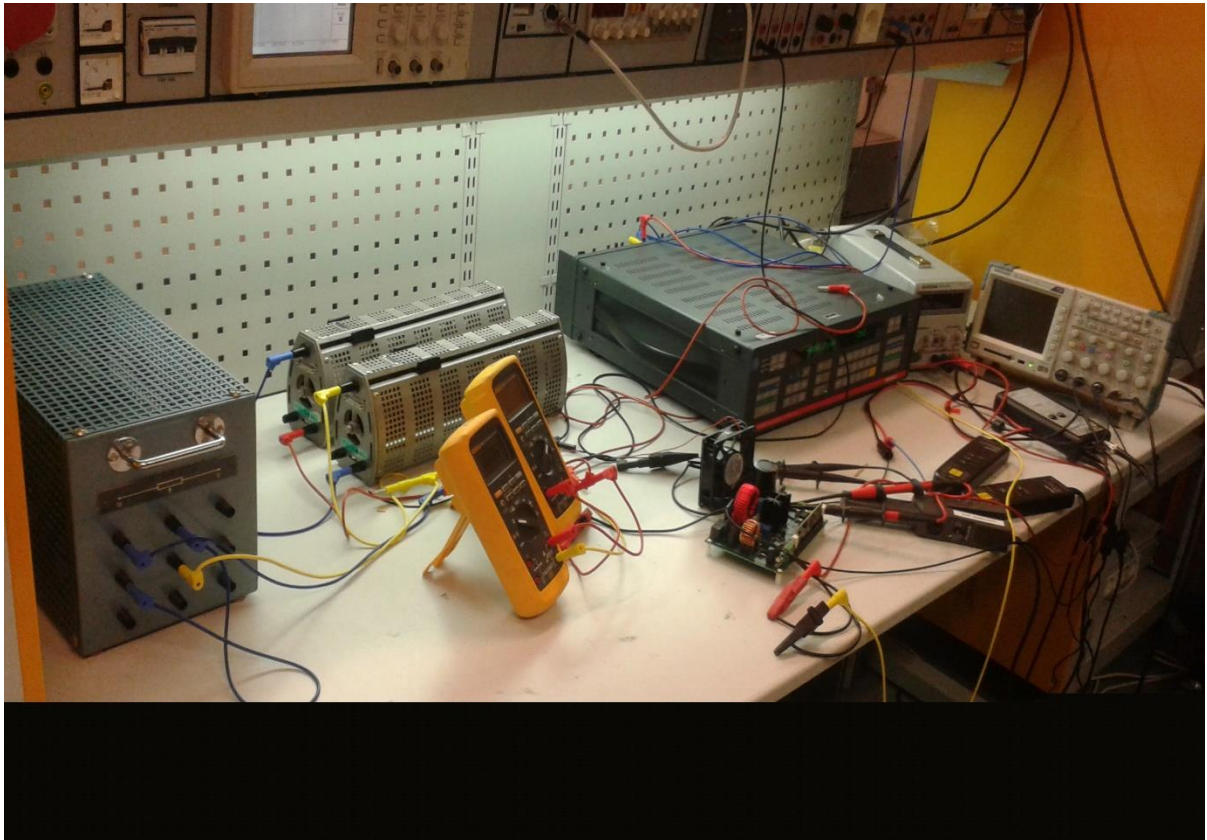
Conventionally diodes were being used in rectifier portion. As mentioned earlier, a full bridge or center taped transformer with two diodes can be employed to rectify the sinusoidal current from resonant tank. However, forward drop of diodes contribute significant amount of power losses that is why in order to improve the efficiency of overall circuit diodes were being replaced with Si MOSFETs. These silicon FETs are switched simultaneously with primary side switching devices. However, for switching frequency  $f_p < f_s > f_o$ , the use of FETs on secondary side becomes

dangerous. As for this frequency range, there exists a dead region in magnetization current during which no energy gets transferred from primary to secondary side. During that short interval, heavy current from output bulk capacitor may flow through the body of rectifier MOSFET and it will completely damage the whole converter. In order to avoid the dead region and get triangular magnetization current, converter with FETs in rectifier are operated at switching frequency in the range of  $f_s > f_o$ .

## Chapter 5. Experimental Measurements and results:

### 5.1 Totem Pole PFC Measurements:

Totem Pole PFC topology has been discussed in detail in section 3.5.3. In this section experimental results obtained from evaluation of Transphorm Totem Pole PFC evaluation kit will be presented.



*Figure 68: Lab setup for totem pole PFC*

Figure 68 shows the lab setup that has been used for the evaluation of Totem Pole PFC circuit. As per instructions of manufacturer, only resistive load was applied to the circuit. This technology is yet not mature enough to handle inductive loads.

Before applying 230 VAC, circuit was first tested at low input voltage. At low voltage gate driver of switches will not operate and circuit should behave as a diode bridge.

In both Figure 69 & Figure 70 CH 1 gives us voltage  $V_D$ . Measuring point for voltage  $V_D$  can be seen in Figure 43. CH2 and CH3 gives us the input current and inductive current respectively.

As input voltage is increased to 230 VAC, control circuit starts operating.

Figure 71 & Figure 72 shows the switching ON and off of GaN HEMT. As it can also be seen in the figures, rise time of 161 ns and fall time of 151 ns was being measured.

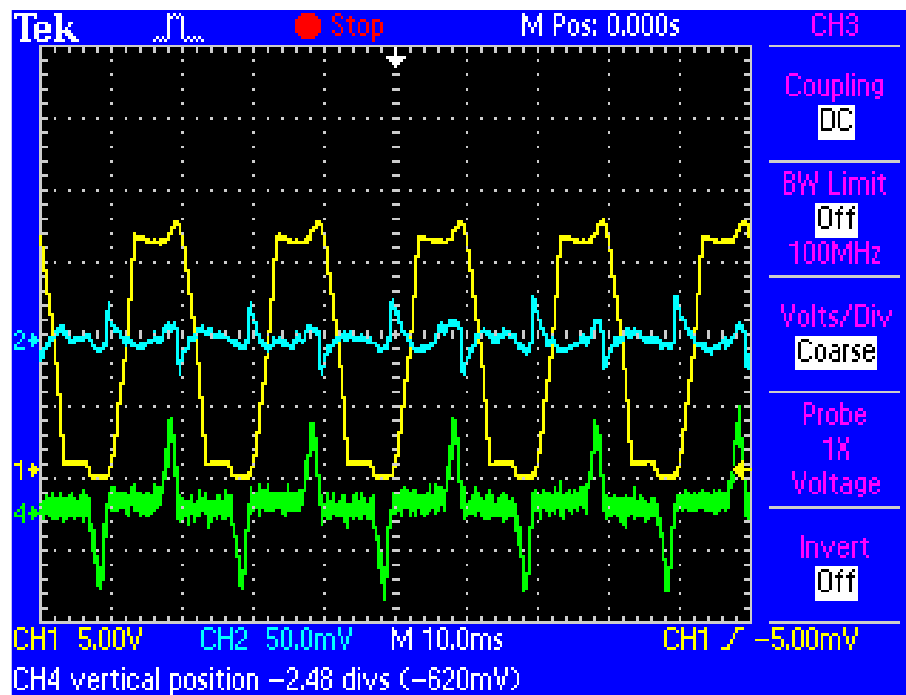


Figure 69: Waveforms at 22 VAC input voltage

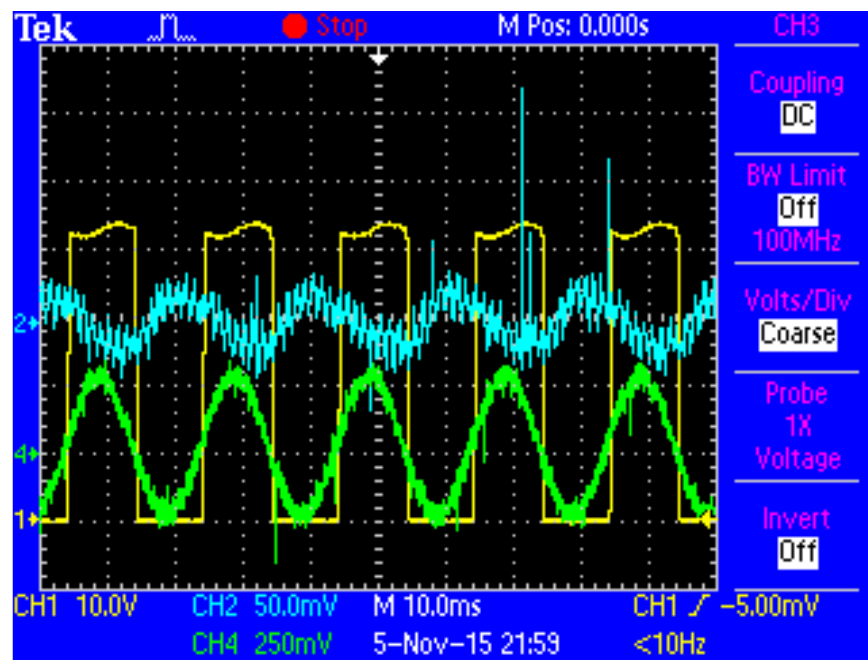


Figure 70: Waveforms at 230 VAC

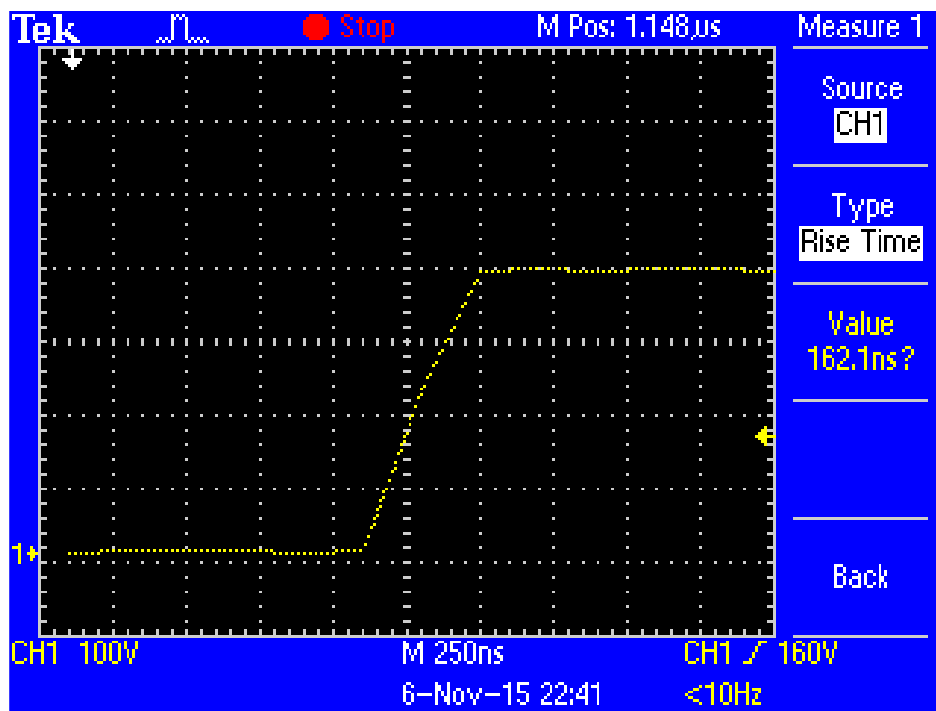


Figure 71: Switching ON of GaN HEMT

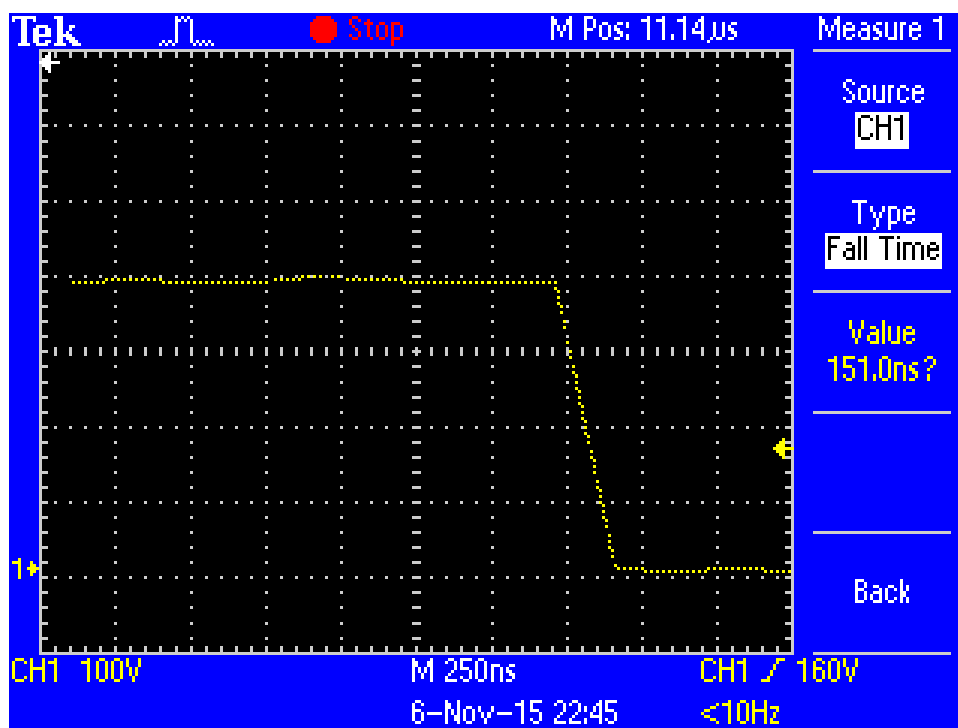


Figure 72: Switching OFF of GaN HEMT

As explained in section 3.5.3, realization of totem pole PFC was not possible with conventional Si power switches. Large reverse recovery for Si switches makes this topology infeasible.

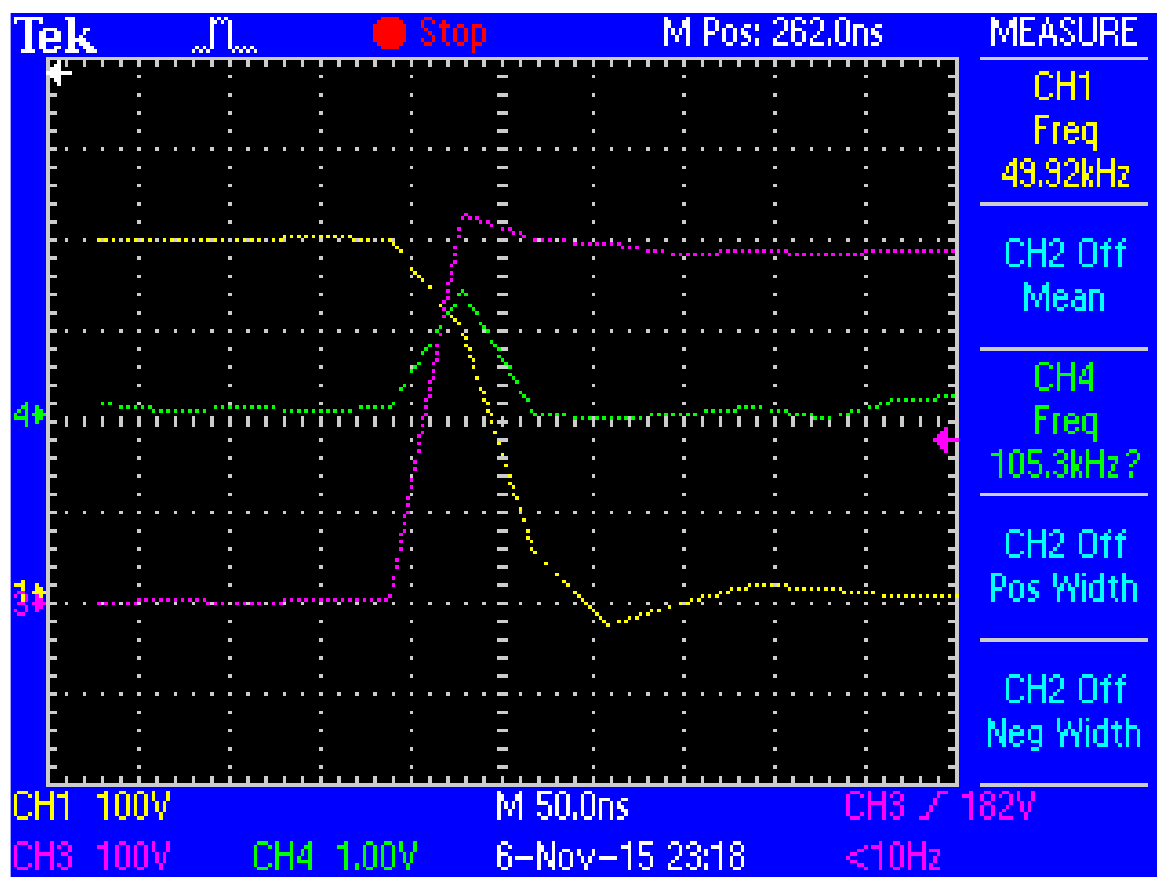


Figure 73: Reverse Recovery characteristics of GaN HEMTs

CH1 and CH3 shows the switching transition of both switches in totem pole. CH4 shows the current through inductor. This small rise in inductor current during switching transition is due to the short circuit created by the switches. However, these switches are very fast with very small reverse recovery that losses due to this short circuit will be negligible. Had this circuit been implemented by slow Si switches, these losses would have made this circuit infeasible and uneconomical.

Charging and discharging of inductor current can be visualized by Figure 74. It can be seen that inductor was always in continuous conduction mode.

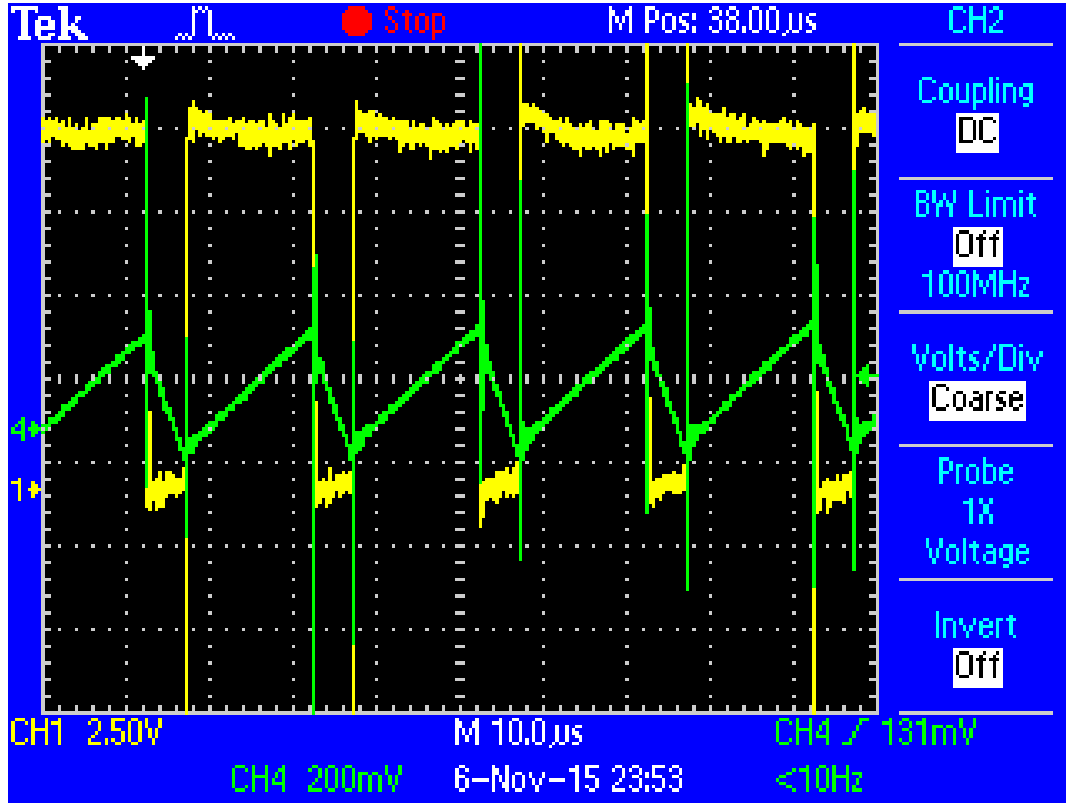


Figure 74: Charging and Discharging of Inductor Current

Power analyzer has been used in our lab to measure the input power factor and power for efficiency calculations. Measurements were taken under different loading conditions. Input voltage for all measurements was 230 VAC while output voltage was fixed at 388.2 VDC.

Table 6: Efficiency of Totem Pole PFC Evaluation Board under different loading conditions

| $I_{IN}$ | $I_{OUT}$ | Pf     | $P_{IN}$ | $P_{OUT}$ | Efficiency (%) |
|----------|-----------|--------|----------|-----------|----------------|
| 0.70     | 0.38      | 0.9901 | 150.22   | 148.68    | 98.98          |
| 1.12     | 0.65      | 0.9915 | 254.30   | 251.55    | 98.92          |
| 1.40     | 0.81      | 0.9927 | 317.20   | 313.67    | 98.89          |
| 1.78     | 1.03      | 0.9932 | 401.90   | 397.91    | 99.01          |
| 2.28     | 1.30      | 0.9941 | 508.50   | 503.11    | 98.94          |
| 2.73     | 1.55      | 0.9943 | 608.00   | 600.16    | 98.71          |
| 3.18     | 1.81      | 0.9943 | 711.00   | 702.64    | 98.82          |
| 3.67     | 2.08      | 0.9940 | 815.80   | 805.90    | 98.79          |
| 4.11     | 2.31      | 0.9945 | 907.00   | 895.58    | 98.74          |

## 5.2 All in One Power Supply Measurements:

Transphorm with collaboration of ON semiconductor released this 12 V / 250 W demo design of all GaN based power supply. This power supply has a bridged PFC Circuit followed by resonant LLC half bridge circuit and synchronous rectifier which have been discussed in detail in Chapter 3 & Chapter 4.

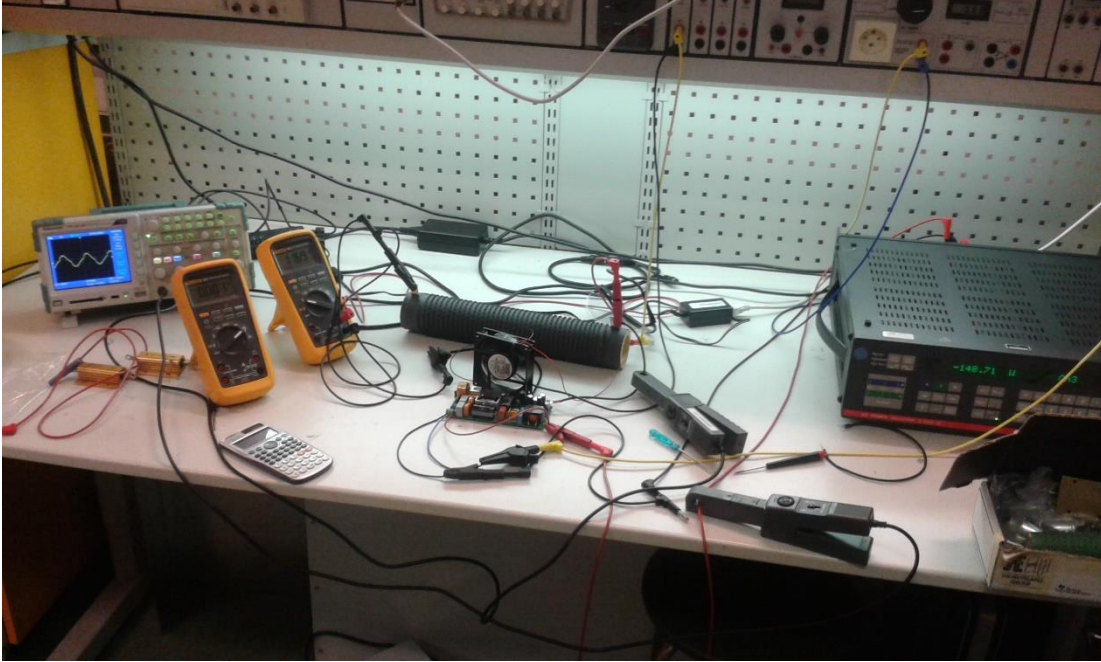


Figure 75: Lab setup for evaluation of All in one Power Supply

Efficiency of power supply was being measured under different loading conditions for fixed input voltage of 220 VAC.

Table 7: Efficiency of All in One Power Supply under different loading conditions

| $V_{OUT}$ | $I_{IN}$ | $I_{OUT}$ | Pf     | $P_{IN}$ | $P_{OUT}$ | Efficiency (%) |
|-----------|----------|-----------|--------|----------|-----------|----------------|
| 11.93     | 0.12     | 1.20      | 0.6775 | 17.11    | 14.30     | 83.60          |
| 11.86     | 0.14     | 1.82      | 0.8050 | 24.61    | 21.59     | 87.71          |
| 11.65     | 0.24     | 3.58      | 0.8977 | 46.25    | 41.68     | 90.13          |
| 11.46     | 0.32     | 5.09      | 0.9450 | 65.16    | 58.33     | 89.52          |
| 11.67     | 0.71     | 12.10     | 0.9754 | 149.77   | 141.21    | 94.28          |
| 11.11     | 0.81     | 13.84     | 0.9780 | 172.01   | 153.76    | 89.39          |
| 10.85     | 1.06     | 18.10     | 0.9791 | 225.48   | 196.39    | 87.10          |



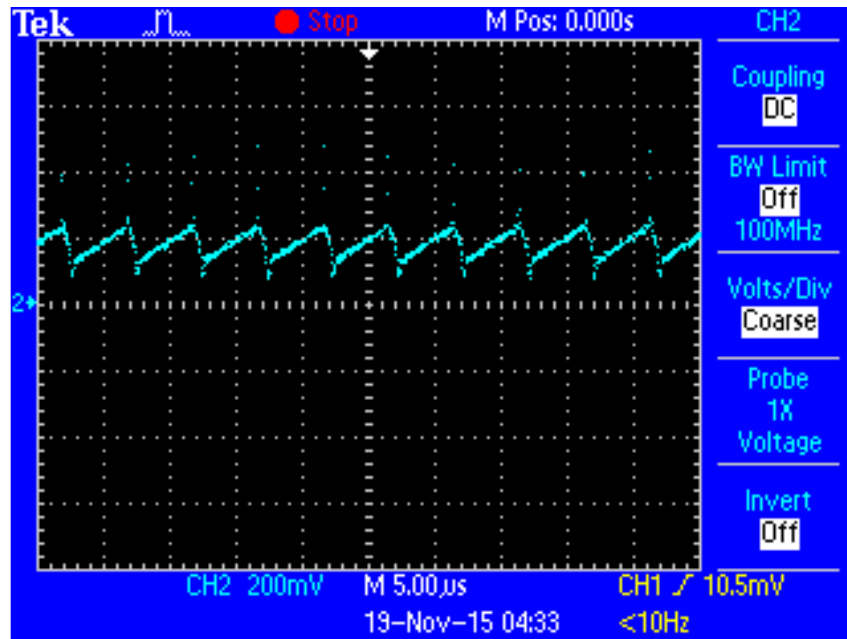


Figure 76: Charging and discharging of Boost Inductor

Current through boost current was observed for output current of 18 A. Ramping up and down of current without touching the zero level in Figure 76 shows CCM operation of boost PFC circuit.

Input current waveform was also being observed.

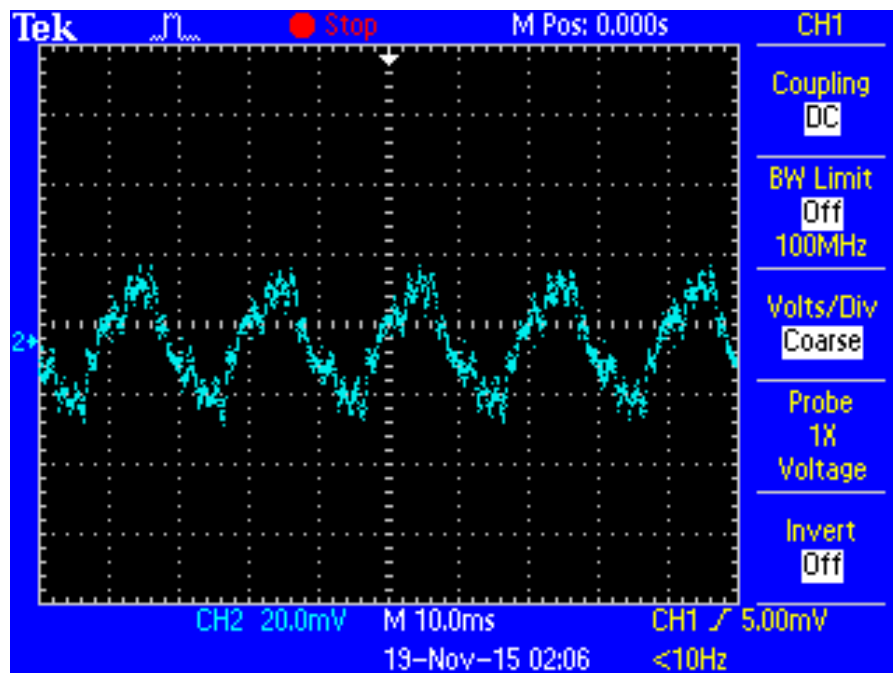
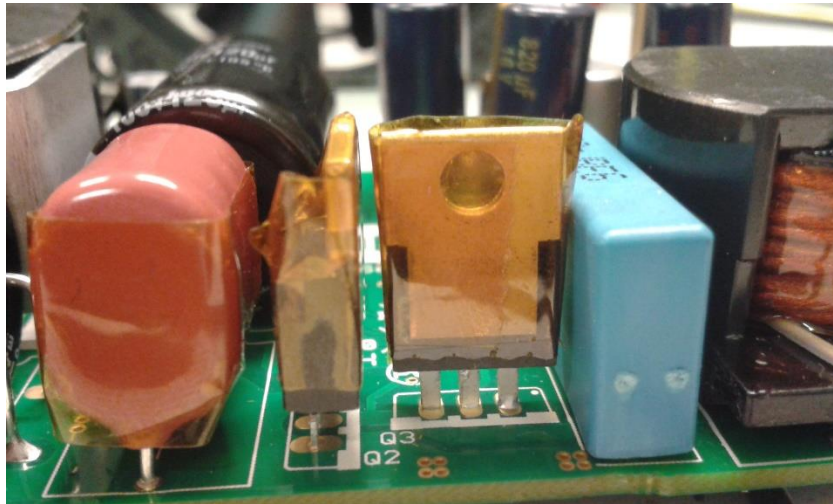


Figure 77: Input Current Waveform @ 14.33 W / 0.6775 Pf

Evaluation of resonant circuit could not be performed because of compact design of evaluation board.



*Figure 78: Compact design of Evaluation Board*

## Chapter 6. Conclusion

WBG power semiconductor devices have started taking hold of power electronics industry. Excellent results with improved over all efficiency, power density have been achieved by employing WBG devices that were considered to be unachievable with conventional Si devices. WBG devices especially SiC devices are mature enough to be used in industrial applications. High voltage applications including electrical vehicles and railway traction systems are considered to be ideal applications for SiC devices. However, GaN power devices are still in development phase. GaN devices especially HEMTs are employed in PFC circuits and power supplies to get improved performance.

If we talk about reliability of WBG devices, then there is still a big question mark. These devices usually suffer from phenomena including body diode degradation, gate threshold voltage shifting. Efforts are being made to develop more reliable devices. Reliability is not the only phenomena undermining performance of WBG devices. Packaging of devices is another major hurdle in the path of these devices. WBG materials are capable of operating at high ambient temperatures and high switching frequencies. But unavailability of proper packaging material puts a limit on operating temperature on these devices. Apart from packaging materials, new packaging technologies with low parasitic inductances are required for high frequency operation of power devices.

PFC circuit is one of the major applications of WBG devices. Especially GaN HEMTs and SiC diodes are generating a lot of revenue from DC power supplies. Simulation of single phase bridged PFC circuit revealed that GaN HEMT along with SiC diode is indeed a best choice for PFC circuit. However, due to fast response of GaN HEMTs ringing effect was observed. It calls for improvement in parasitics of circuit elements. Simulation results also revealed the need of fast drivers for these new devices.

Power factor data from Table 6 & Table 7 gives the comparison of performance of two different topologies of PFC circuit. It can be seen in Table 6 that even for low loads power factor of totem pole PFC was greater than 0.99. However, Table 7 reveals the poor performance of bridged PFC circuits at low load conditions.

Next phase of this project will be to implement single phase bridged PFC circuit on hardware level. Comparison of practical results will be made with simulated results for all three switches. Another future dimension of this research can be to develop a faster driver circuit for PFC circuit used in simulation.

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## Appendix A:

### Calculation for Sensing Resistor:

All design equations are taken from (Linear Technology 1994)

$$I_{LMAX} = I_{MMAX} \cdot \frac{R_{REF}}{R_s}$$

For  $R_{SET}$  of 15 k $\Omega$ ,

$$I_{MMAX} = \frac{3.75}{R_{SET}} = 250 \mu A$$

If  $R_{REF}$  is set to 4 k $\Omega$  then for maximum line current limit of 5 A value of sensing resistance should be:

$$R_s = I_{MMAX} \cdot \frac{R_{REF}}{I_{LMAX}} = 0.2 \Omega$$

### Output Voltage Divider Circuit:

$$V_{out} = \frac{R_2}{R_1 + R_2} * V_{In}$$

As in our case:

$$V_{out} = 7.5V$$

$$V_{In} = 400V$$

If we chose value of  $R_1$  to be 1Meg $\Omega$

$$R_2 = \frac{V_{out} R_1}{V_{In} - V_{out}} = 19.10k\Omega$$

## Appendix B:

transphorm

TPH3002PS

### PRODUCT SUMMARY (TYPICAL)

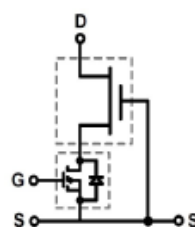
|                           |      |
|---------------------------|------|
| $V_{DS}$ (V)              | 600  |
| $R_{DS(on)}$ ( $\Omega$ ) | 0.29 |
| $Q_{rr}$ (nC)             | 29   |

#### Features

- Low  $Q_{rr}$
- Free-wheeling diode not required
- Low-side Quiet Tab™ for reduced EMI
- GSD pin layout improves high speed design
- RoHS compliant

#### Applications

- High frequency operation
- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies



TO-220 Package

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise stated)

| Symbol                   | Parameter   | Limit Value | Unit             |
|--------------------------|---|-------------|------------------|
| $I_{D25^\circ\text{C}}$  | Continuous Drain Current @ $T_C=25^\circ\text{C}$     | 9           | A                |
| $I_{D100^\circ\text{C}}$ | Continuous Drain Current @ $T_C=100^\circ\text{C}$    | 6           | A                |
| $I_{DM}$                 | Pulsed Drain Current (pulse width:100 $\mu\text{s}$ ) | 33          | A                |
| $V_{DS}$                 | Drain to Source Voltage                               | 600         | V                |
| $V_{TDS}$                | Transient Drain to Source Voltage <sup>a</sup>        | 750         | V                |
| $V_{GS}$                 | Gate to Source Voltage                                | $\pm 18$    | V                |
| $P_{D25^\circ\text{C}}$  | Maximum Power Dissipation                             | 65          | W                |
| $T_C$                    | Operating Temperature Case                            | -55 to 150  | $^\circ\text{C}$ |
| $T_J$                    | Junction  | -55 to 175  | $^\circ\text{C}$ |
| $T_S$                    | Storage Temperature                                   | -55 to 150  | $^\circ\text{C}$ |
| $T_{Csold}$              | Soldering peak Temperature <sup>b</sup>               | 260         | $^\circ\text{C}$ |

### Thermal Resistance

| Symbol          | Parameter           | Typical | Unit               |
|-----------------|---------------------|---------|--------------------|
| $R_{\theta JC}$ | Junction-to-Case    | 2.3     | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Junction-to-Ambient | 62      | $^\circ\text{C/W}$ |

#### Notes

a: For 1 usec, duty cycle D=0.1

b: For 10 sec, 1.6mm from the case

TPH3002PS

[www.transphormusa.com](http://www.transphormusa.com)

January 26, 2015, JH

1

| Electrical Characteristics (T <sub>C</sub> =25°C* unless otherwise stated) |   |      |         |      |      |  |
|--|---|------|---------|------|------|--|
| Symbol   | Parameter   | Min  | Typical | Max  | Unit | Test Conditions  |
| Static   |   |      |         |      |      |  |
| V <sub>DS-MAX</sub>  | Maximum Drain-Source Voltage                            | 600  |         |      | V    | V <sub>GS</sub> =0V  |
| V <sub>GS(th)</sub>  | Gate Threshold Voltage                                  | 1.35 | 1.8     | 2.35 | V    | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =25 μA                                       |
| R <sub>DS(on)</sub>  | Drain-Source On-Resistance (T <sub>J</sub> = 25°C)      | -    | 0.29    | 0.35 | Ω    | V <sub>GS</sub> =8V, I <sub>D</sub> = 5.5A, T <sub>J</sub> = 25°C                              |
| R <sub>DS(on)</sub>  | Drain-Source On-Resistance (T <sub>J</sub> = 175°C)     | -    | 0.76    |      | Ω    | V <sub>GS</sub> =8V, I <sub>D</sub> = 5.5A, T <sub>J</sub> = 175°C                             |
| I <sub>DSS</sub>   | Drain-to-Source Leakage Current, T <sub>J</sub> = 25°C  | -    | 2.5     | 60   | μA   | V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> = 25°C                              |
| I <sub>DSS</sub>   | Drain-to-Source Leakage Current, T <sub>J</sub> = 150°C | -    | 10      |      | μA   | V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> = 150°C                             |
| Dynamic  |   |      |         |      |      |  |
| C <sub>iss</sub>   | Input Capacitance                                       | -    | 785     | -    | pF   | V <sub>GS</sub> =0 V, V <sub>DS</sub> =400V, f = 1 MHz   |
| C <sub>OSS</sub>   | Output Capacitance                                      | -    | 26      | -    |      |  |
| C <sub>RSS</sub>   | Reverse Transfer Capacitance                            | -    | 3.5     | -    |      |  |
| C <sub>O(er)</sub>   | Output Capacitance, energy related                      | -    | 36      | -    |      | V <sub>GS</sub> =0 V, V <sub>DS</sub> =0 V to 480 V  |
| C <sub>O(tr)</sub>   | Output Capacitance, time related                        | -    | 63      | -    |      |  |
| Q <sub>g</sub>   | Total Gate Charge                                       | -    | 6.2     | 9.3  | nC   | V <sub>DS</sub> =100 V <sup>c</sup> , V <sub>GS</sub> = 0-4.5 V, I <sub>D</sub> = 5.5A         |
| Q <sub>gs</sub>  | Gate-Source Charge                                      | -    | 2.1     | -    |      |  |
| Q <sub>gd</sub>  | Gate-Drain Charge                                       | -    | 2.2     | -    |      |  |
| t <sub>d(on)</sub>   | Turn-On Delay   |      | 7.5     |      | ns   | V <sub>DS</sub> =480 V, V <sub>GS</sub> = 0-10 V, I <sub>D</sub> = 5.5 A, R <sub>θ</sub> = 2 Ω |
| t <sub>r</sub>   | Rise Time   |      | 4       |      |      |  |
| T <sub>d(off)</sub>  | Turn-Off Delay  |      | 10      |      |      |  |
| t <sub>f</sub>   | Fall Time   |      | 4.5     |      |      |  |
| Reverse operation  |   |      |         |      |      |  |
| I <sub>S</sub>   | Reverse Current   | -    | -       | 12   | A    | V <sub>GS</sub> =0 V, T <sub>J</sub> =100°C, Duty=5%, >10kHz                                   |
| V <sub>SD</sub>  | Reverse Voltage   | -    | 2.3     | 2.9  | V    | V <sub>GS</sub> =0 V, I <sub>S</sub> =6A, T <sub>J</sub> =25°C, Duty=10%, >10 kHz              |
| V <sub>SD</sub>  | Reverse Voltage   | -    | 1.8     | 2.3  | V    | V <sub>GS</sub> =0 V, I <sub>S</sub> =3A, T <sub>J</sub> =25°C, Duty=10%, >10 kHz              |
| t <sub>rr</sub>  | Reverse Recovery Time                                   | -    | 30      |      | ns   | I <sub>S</sub> =5.5A, V <sub>DO</sub> =480 V, di/dt =450 A/μs, T <sub>J</sub> =25°C            |
| Q <sub>rr</sub>  | Reverse Recovery Charge                                 | -    | 29      |      | nC   |  |

**Notes**

c: Q<sub>g</sub> does not change for V<sub>DS</sub>>100 V

## Appendix C:



### C2M0280120D

#### Silicon Carbide Power MOSFET

#### C2M™ MOSFET Technology

#### N-Channel Enhancement Mode

##### Features

- New C2M SiC MOSFET technology
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

##### Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

##### Applications

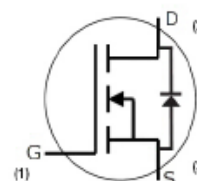
- LED Lighting Power Supplies
- High Voltage DC/DC Converters
- Industrial Power Supplies
- HVAC

|                          |        |
|--------------------------|--------|
| $V_{DS}$                 | 1200 V |
| $I_D @ 25^\circ\text{C}$ | 10 A   |
| $R_{DS(on)}$             | 280 mΩ |

##### Package



TO-247-3



| Part Number | Package  |
|-------------|----------|
| C2M0280120D | TO-247-3 |

##### Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

| Symbol         | Parameter                                  | Value       | Unit             | Test Conditions                                     | Note    |
|----------------|--|-------------|------------------|---|---------|
| $V_{DSmax}$    | Drain - Source Voltage                     | 1200        | V                | $V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$ |         |
| $V_{GSmax}$    | Gate - Source Voltage                      | -10/+25     | V                | Absolute maximum values                             |         |
| $V_{GSop}$     | Gate - Source Voltage                      | -5/+20      | V                | Recommended operational values                      |         |
| $I_D$          | Continuous Drain Current                   | 10          | A                | $V_{GS} = 20\text{ V}, T_C = 25^\circ\text{C}$      | Fig. 19 |
|                |  | 6           |                  | $V_{GS} = 20\text{ V}, T_C = 100^\circ\text{C}$     |         |
| $I_{D(pulse)}$ | Pulsed Drain Current                       | 20          | A                | Pulse width $t_p$ limited by $T_{jmax}$             | Fig. 22 |
| $P_D$          | Power Dissipation                          | 62.5        | W                | $T_C = 25^\circ\text{C}, T_J = 150^\circ\text{C}$   | Fig. 20 |
| $T_J, T_{stg}$ | Operating Junction and Storage Temperature | -55 to +150 | $^\circ\text{C}$ |   |         |
| $T_L$          | Solder Temperature                         | 260         | $^\circ\text{C}$ | 1.6 mm (0.063") from case for 10s                   |         |
| $M_d$          | Mounting Torque                            | 1<br>8.8    | Nm<br>lbf-in     | M3 or 6-32 screw                                    |         |



## Electrical Characteristics ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

| Symbol        | Parameter                        | Min. | Typ. | Max. | Unit          | Test Conditions  | Note       |
|---------------|----------------------------------|------|------|------|---------------|--|------------|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage   | 1200 |      |      | V             | $V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$  |            |
| $V_{GS(th)}$  | Gate Threshold Voltage           | 2.4  | 2.8  |      | V             | $V_{DS} = 10\text{ V}, I_D = 1.25\text{ mA}$   | Fig. 11    |
|               |                                  | 1.8  | 2.1  |      | V             | $V_{DS} = 10\text{ V}, I_D = 1.25\text{ mA}, T_j = 150^\circ\text{C}$  |            |
| $I_{DSS}$     | Zero Gate Voltage Drain Current  |      | 1    | 100  | $\mu\text{A}$ | $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$  |            |
| $I_{GSS}$     | Gate-Source Leakage Current      |      |      | 250  | nA            | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$  |            |
| $R_{DS(on)}$  | Drain-Source On-State Resistance |      | 280  | 370  | m $\Omega$    | $V_{GS} = 20\text{ V}, I_D = 6\text{ A}$   | Fig. 4,5,6 |
|               |                                  |      | 530  |      |               | $V_{GS} = 20\text{ V}, I_D = 6\text{ A}, T_j = 150^\circ\text{C}$  |            |
| $g_m$         | Transconductance                 |      | 2.8  |      | S             | $V_{DS} = 20\text{ V}, I_{DS} = 6\text{ A}$  | Fig. 7     |
|               |                                  |      | 2.4  |      |               | $V_{DS} = 20\text{ V}, I_{DS} = 6\text{ A}, T_j = 150^\circ\text{C}$   |            |
| $C_{iss}$     | Input Capacitance                |      | 259  |      |               | $V_{GS} = 0\text{ V}$<br>$V_{DS} = 1000\text{ V}$<br>$f = 1\text{ MHz}$<br>$V_{AC} = 25\text{ mV}$   | Fig. 17,18 |
| $C_{oss}$     | Output Capacitance               |      | 23   |      | pF            |  |            |
| $C_{rss}$     | Reverse Transfer Capacitance     |      | 3    |      |               |  |            |
| $E_{oss}$     | $C_{oss}$ Stored Energy          |      | 12.5 |      | $\mu\text{J}$ |  |            |
| $E_{AS}$      | Avalanche Energy, Single Pulse   |      | 280  |      | mJ            | $I_D = 6\text{ A}, V_{DS} = 50\text{ V}$   | Fig. 29    |
| $E_{ON}$      | Turn-On Switching Energy         |      | 32   |      | $\mu\text{J}$ | $V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$<br>$I_D = 6\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 412\text{ }\mu\text{H}$   | Fig. 25    |
| $E_{OFF}$     | Turn Off Switching Energy        |      | 37   |      |               |  |            |
| $t_{d(on)}$   | Turn-On Delay Time               |      | 5.2  |      | ns            | $V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$<br>$I_D = 6\text{ A}$<br>$R_{G(ext)} = 2.5\text{ }\Omega, R_L = 133\text{ }\Omega$<br>Timing relative to $V_{DS}$<br>Per IEC60747-8-4 pg 83 | Fig. 27    |
| $t_r$         | Rise Time                        |      | 7.6  |      |               |  |            |
| $t_{d(off)}$  | Turn-Off Delay Time              |      | 10.8 |      |               |  |            |
| $t_f$         | Fall Time                        |      | 9.9  |      |               |  |            |
| $R_{GS(int)}$ | Internal Gate Resistance         |      | 11.4 |      | $\Omega$      | $f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$ , ESR of $C_{iss}$   |            |
| $Q_{gs}$      | Gate to Source Charge            |      | 5.6  |      | nC            | $V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$<br>$I_D = 6\text{ A}$<br>Per IEC60747-8-4 pg 21   | Fig. 12    |
| $Q_{gd}$      | Gate to Drain Charge             |      | 7.6  |      |               |  |            |
| $Q_g$         | Gate Charge Total                |      | 20.4 |      |               |  |            |

## Reverse Diode Characteristics

| Symbol    | Parameter                        | Typ. | Max. | Unit | Test Conditions  | Note          |
|-----------|----------------------------------|------|------|------|--|---------------|
| $V_{SD}$  | Diode Forward Voltage            | 3.3  |      | V    | $V_{GS} = -5\text{ V}, I_{SD} = 3\text{ A}$  | Fig. 8, 9, 10 |
|           |                                  | 3.1  |      | V    | $V_{GS} = -5\text{ V}, I_{SD} = 3\text{ A}, T_j = 150^\circ\text{C}$                                   |               |
| $I_S$     | Continuous Diode Forward Current |      | 10   | A    | $T_c = 25^\circ\text{C}$   | Note 1        |
| $t_{rr}$  | Reverse Recovery time            | 24   |      | ns   | $V_{GS} = -5\text{ V}, I_{SD} = 6\text{ A}, V_R = 800\text{ V}$<br>$di/dt = 1000\text{ A}/\mu\text{s}$ | Note 1        |
| $Q_{rr}$  | Reverse Recovery Charge          | 70   |      | nC   |  |               |
| $I_{rrm}$ | Peak Reverse Recovery Current    | 4    |      | A    |  |               |

Note (1): When using SiC Body Diode the maximum recommended  $V_{GS} = -5\text{ V}$

## Thermal Characteristics

| Symbol          | Parameter                                   | Typ. | Max. | Unit                      | Test Conditions | Note    |
|-----------------|---|------|------|---------------------------|-----------------|---------|
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case    | 1.8  | 2.0  | $^\circ\text{C}/\text{W}$ |                 | Fig. 21 |
| $R_{\theta JA}$ | Thermal Resistance from Junction to Ambient |      | 40   |                           |                 |         |

## Appendix D:



### SPP11N60C3, SPI11N60C3, SPA11N60C3, SPA11N60C3 E8185

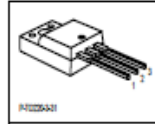
#### Cool MOS™ Power Transistor

##### Feature

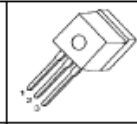
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme  $dv/dt$  rated
- High peak current capability
- Improved transconductance
- PG-TO-220-3-31;-3-111: Fully isolated package (2500 VAC; 1 minute)
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>(1)</sup> for target applications

|                     |      |          |
|---------------------|------|----------|
| $V_{DS} @ T_{jmax}$ | 650  | V        |
| $R_{DS(on)}$        | 0.38 | $\Omega$ |
| $I_D$               | 11   | A        |

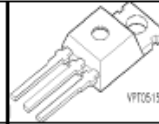
PG-TO220FP



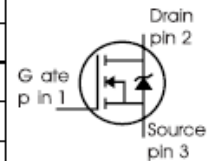
PG-TO262



PG-TO220



| Type            | Package    | Ordering Code | Marking |
|-----------------|------------|---------------|---------|
| SPP11N60C3      | PG-TO220   | Q67040-S4395  | 11N60C3 |
| SPI11N60C3      | PG-TO262   | Q67042-S4403  | 11N60C3 |
| SPA11N60C3      | PG-TO220FP | Q67040-S4408  | 11N60C3 |
| SPA11N60C3E8185 | PG-TO220   |               | 11N60C3 |



#### Maximum Ratings

| Parameter   | Symbol               | Value      |                                     | Unit             |
|---|----------------------|------------|-------------------------------------|------------------|
|   |                      | SPP 1      | SPA                                 |                  |
| Continuous drain current<br>$T_C = 25^\circ\text{C}$<br>$T_C = 100^\circ\text{C}$                                   | $I_D$                | 11<br>7    | 11 <sup>1)</sup><br>7 <sup>1)</sup> | A                |
| Pulsed drain current, $t_p$ limited by $T_{jmax}$   | $I_{D \text{ puls}}$ | 33         | 33                                  | A                |
| Avalanche energy, single pulse<br>$I_D=5.5\text{A}$ , $V_{DD}=50\text{V}$   | $E_{AS}$             | 340        | 340                                 | mJ               |
| Avalanche energy, repetitive $t_{AR}$ limited by $T_{jmax}$ <sup>2)</sup><br>$I_D=11\text{A}$ , $V_{DD}=50\text{V}$ | $E_{AR}$             | 0.6        | 0.6                                 |                  |
| Avalanche current, repetitive $t_{AR}$ limited by $T_{jmax}$  | $I_{AR}$             | 11         | 11                                  | A                |
| Gate source voltage static  | $V_{GS}$             | $\pm 20$   | $\pm 20$                            | V                |
| Gate source voltage AC ( $f > 1\text{Hz}$ )   | $V_{GS}$             | $\pm 30$   | $\pm 30$                            |                  |
| Power dissipation, $T_C = 25^\circ\text{C}$   | $P_{tot}$            | 125        | 33                                  | W                |
| Operating and storage temperature   | $T_j, T_{stg}$       | -55...+150 |                                     | $^\circ\text{C}$ |
| Reverse diode $dv/dt$ <sup>7)</sup>   | $dv/dt$              | 15         |                                     | V/ns             |

#### Maximum Ratings

| Parameter   | Symbol  | Value | Unit |
|---|---------|-------|------|
| Drain Source voltage slope<br>$V_{DS} = 480\text{ V}, I_D = 11\text{ A}, T_j = 125^\circ\text{C}$ | $dv/dt$ | 50    | V/ns |

#### Thermal Characteristics

| Parameter   | Symbol         | Values |         |         | Unit |
|---|----------------|--------|---------|---------|------|
|   |                | min.   | typ.    | max.    |      |
| Thermal resistance, junction - case   | $R_{thJC}$     | -      | -       | 1       | K/W  |
| Thermal resistance, junction - case, FullPAK  | $R_{thJC\_FP}$ | -      | -       | 3.8     |      |
| Thermal resistance, junction - ambient, leaded  | $R_{thJA}$     | -      | -       | 62      |      |
| Thermal resistance, junction - ambient, FullPAK   | $R_{thJA\_FP}$ | -      | -       | 80      |      |
| SMD version, device on PCB:<br>@ min. footprint<br>@ 6 cm <sup>2</sup> cooling area <sup>3)</sup> | $R_{thJA}$     | -<br>- | -<br>35 | 62<br>- |      |
| Soldering temperature, wavesoldering<br>1.6 mm (0.063 in.) from case for 10s <sup>4)</sup>        | $T_{solder}$   | -      | -       | 260     | °C   |

#### Electrical Characteristics, at $T_j=25^\circ\text{C}$ unless otherwise specified

| Parameter                                | Symbol        | Conditions   | Values |              |           | Unit          |
|--|---------------|--|--------|--------------|-----------|---------------|
|  |               |  | min.   | typ.         | max.      |               |
| Drain-source breakdown voltage           | $V_{(BR)DSS}$ | $V_{GS}=0\text{V}, I_D=0.25\text{mA}$  | 600    | -            | -         | V             |
| Drain-Source avalanche breakdown voltage | $V_{(BR)DS}$  | $V_{GS}=0\text{V}, I_D=11\text{A}$   | -      | 700          | -         |               |
| Gate threshold voltage                   | $V_{GS(th)}$  | $I_D=500\mu\text{A}, V_{GS}=V_{DS}$  | 2.1    | 3            | 3.9       |               |
| Zero gate voltage drain current          | $I_{DSS}$     | $V_{DS}=600\text{V}, V_{GS}=0\text{V},$<br>$T_j=25^\circ\text{C}$<br>$T_j=150^\circ\text{C}$ | -<br>- | 0.1<br>-     | 1<br>100  | $\mu\text{A}$ |
| Gate-source leakage current              | $I_{GSS}$     | $V_{GS}=30\text{V}, V_{DS}=0\text{V}$  | -      | -            | 100       | nA            |
| Drain-source on-state resistance         | $R_{DS(on)}$  | $V_{GS}=10\text{V}, I_D=7\text{A}$<br>$T_j=25^\circ\text{C}$<br>$T_j=150^\circ\text{C}$      | -<br>- | 0.34<br>0.92 | 0.38<br>- | $\Omega$      |
| Gate input resistance                    | $R_G$         | $f=1\text{MHz}, \text{open drain}$   | -      | 0.86         | -         |               |